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A New Interleaved ZVT High Step-Up Converter with Low Count Elements for Photovoltaic Applications

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ABSTRACT

A new interleaved high step-up converter with Zero Voltage Transition (ZVT) is proposed for operation in this paper. The main advantages of the proposed converter are low input current ripple and low voltage stress on the power switches, high efficiency, low total component count, and eliminating reverse recovery problem of power diodes. Due to the soft switching operation of the switches and diodes in the converter, the efficiency has been enhanced. Also, the switches do not have capacitive turn on loss due to ZVT operation. The proposed converter uses only one power switch to provide ZVT conditions for all switches and the clamp capacitor transfers its energy to the lifting capacitor, which causes increase in voltage gain of the converter. Because of the interleaved structure, the converter has a low input ripple current and this advantage makes it very suitable for solar applications. The proposed converter is analysed and a 580W prototype is made to verify theoretical analyses.

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1. INTRODUCTION

With the scarcity of fossil fuels and their replacement by green energy sources such as photovoltaic systems, fuel cells, and wind power, not only do greenhouse gas emissions decrease but also the increase in flexibility and reliability in power generation is ensured [1-3]. To maintain DC bus voltage (380-400 V), renewable and distributed generation of the microgrid is essential among the fundamental factors in sustaining high DC bus voltage. In photovoltaic systems, output voltage is low and variable and in order to provide DC line requirements, high step-up DC-DC converters are used widely in the power conversion stage. Besides, to harness greater power, reliability, and efficiency, Photovoltaic arrays are installed with modular DC-DC structures [4-6].

The conventional boost converters have a small number of elements, simple modeling, and design, but have many disadvantages such as high voltage peak on the switch and diode, narrow duty cycle, and reverse recovery problem of the diode. There are several voltage-boosting techniques such as switched capacitors, voltage multiplier, switched inductors or voltage lifting, magnetic coupling, and multistage structures [7-9].

Non-isolated converters often have an uncomplicated structure with lower weight and cost than isolated ones. These converters are not suitable for extracting high power levels. One of the main advantages of these converters is their electrical connections between the input and output and greater efficacy compared to the isolated ones [10-15].

The multiphase interleaved techniques manage to increase power density and reduce input current ripple. Several types of interleaved high step-up converters have been presented recently, which use an auxiliary circuit to recycle leakage inductances energy and provide zero-voltage conditions for the main switches [16-21].

A high step-up interleaved DC-DC converter with ZVT performance was introduced in [18]. An auxiliary circuit including auxiliary switches and clamp capacitors was used to reduce switching losses and control spike voltage of all switches. A transformer with three windings is employed to boost the voltage and reduce the voltage stress of all switches. Leakage inductance controls the current of output diodes and improves the problem of reverse recovery of these diodes. However, the gain of the converter is low. In addition, the voltage of output diode is twice that of output voltage, which is a considerable amount given the operation of this converter at high voltages. The use of two additional switches also may control circuit complexity.

The converter introduced in [19] also uses a combination of coupled inductors with three windings and voltage boosters to provide a high voltage gain converter. This converter, thanks to the use of three coupled inductors and voltage boosters, provides a suitable voltage gain while reducing the voltage stress of its semiconductor elements. If the winding ratio is uniform, its voltage gain will be four times a boost converter. Under such conditions, the voltage across the main switches and clamp diodes is a quarter of the output voltage, and other

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diodes withstand stress equal to Vo/2. However, such a coil structure, called WCCI, is a bit complicated, while the number of elements used in the circuit is relatively large.

Another technique to eliminate switching losses is using the lossless snubber for the switch and the snubber does not impose significant losses on the converter, but the switch drain-source current and voltage stresses increase meaningfully [22-24].

The converters in [25, 26] are interleaved high step-up ones in which an active clamp technique is used to conduct ZV condition. In the main form of the technique, there are two additional switches, duty cycle losses, and high circulating current in the auxiliary circuits.

The converter in [27] is a high step-up converter with switching in zero voltage which applies a new auxiliary circuit with the coupled inductor. The number of elements is relatively large. On the other hand, the coupled inductor in the auxiliary circuit makes the complexity of the converter's operation. Moreover, the driver's circuit should be isolated since the lack of common ground with the source of power MOSFETs. In [21], a high step-up converter with two auxiliary switches was proposed. The major disadvantage of the mentioned circuit is the existence of the auxiliary switch with the floating switch's source. In [21], a high step-up converter using a mini boost converter to recover leakage energy of coupled inductor and transfer it to the load was introduced. The main problem of this converter is the hard switching operation of converter which causes switching losses and limits the switching frequency of the converter. In [28], a new auxiliary circuit for the interleaved converter was introduced. The circuit can be extended to more phases and its energy was transferred to the output in an effective way. However, the critical problems we are facing in this converter are the number of the auxiliary circuit elements as well as use of a coupled inductor in the auxiliary circuit which makes the circuit's operation more complicated.

In [15] and [29], high step-up converters were introduced in which the coupled inductors accompanied with lift voltage capacitors were used to increase voltage gain. The energy in the leakage inductance was absorbed in clamp capacitor. However, in these converters, the soft switching conditions were highly depended on the load. In the light load conditions, the soft switching disappeared and the efficiency was reduced.

In the proposed converter, an active switch was reduced compared to similar ZVT converters, which reduced the conduction losses and the complexity of the circuit operation. Since all switches in the proposed converter operate under ZV condition, unlike ZCS converters, they do not have capacitive turn-on losses.

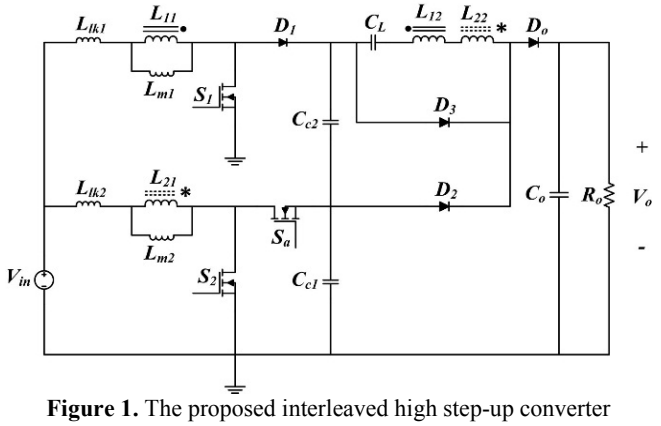

Figure 1. The proposed interleaved high step-up converter

2. THE PROPOSED CONVERTER

2.1. The converter description

The proposed interleaved step-up DC-DC converter with ZVT operation is shown in Figure 1. As shown in the figure, the converter has two main power switches S_1 and S_2 and just an auxiliary switch S_a. Also, capacitors C_{c1} and C_{c2} are used to clamp voltage, the capacitor C_L is employed to lift the voltage gain, and C_o is used to get voltage ripple. To increase the gain, the inductors L_{11}, L_{12}, L_{21}, L_{22} have been coupled, which are modeled by magnetizing inductances L_{m1} and L_{m2} and leakage inductances L_{k1} and L_{k2}, respectively. The converter also includes four diodes D_1, D_2, D_3, and D_o.

2.2. The operation of the proposed high step-up converter

The operation of the proposed converter can be divided into eight operating intervals in a switching cycle. The proposed converter equivalent circuits of the intervals are shown in Figure (2) and the performance of each mode will be examined separately below. The following hypotheses are considered for the simplicity of the proposed converter analysis.

i. The magnetizing inductors are large enough and their current is considered constant in a steady state.
ii. The output and clamp capacitors are designed large enough, and capacitor voltages are assumed to be fixed in a switching cycle.
iii. All semiconductor elements including diodes and switches are modeled ideal.

The main switches are on and the diodes are off before the first mode. The load current is also supplied by the output capacitor and the magnetizing inductances of the converter are charged linearly.

Mode 1 ($t_0<t<t_1$)

This mode starts when S_2 is turned off, and the body diodes of S_a and diode D_o conduct, while the diodes D_1, D_2, and D_3 are off. Therefore, S_a is able to turn on under ZV condition. Also, the leakage inductance energy of L_{lk2} is transmitted through the body diode of S_a to capacitor C_{c1}, and the voltage of switch S_2 is clamped by C_{c1}. On the other hand, when the D_o conducts, the energy of L_{m2} transmits to the output through the secondary side of coupled inductor (L_{22}). The output diode due to the existence of the leakage inductance (L_{lk2}) turns on under ZCS and the currents of L_{m1} and L_{lk1} increase linearly. This mode ends when the L_{lk2} current reaches the secondary winding current (I_{sec}) level.

Mode 2 ($t_1<t<t_2$)

In this state, the current transfers from the anti-parallel diode of S_a to the S_a. In this situation, the current of S_1 continues increasing and the output diode is on. Moreover, only the diode D_o and switches S_1 and S_a conduct and the output is still supplied through capacitors C_{c1}, C_{c2}, and C_L. L_{lk2} current is decreasing with a slight slope and L_{m1} and L_{lk1} currents increase. This state ends when the S_a turns off under ZV condition.

Mode 3 ($t_2<t<t_3$)

When the S_a switch is off, the switch S_2 anti-parallel diode conducts. Therefore, the switch in this interval can be pulsed

under ZV conditions. The leakage current of L_{LK2} increases rapidly, which leads to a decrease in the secondary current. As the leakage current of L_{lk2} reaches the current of L_{m2}, the secondary current goes zero and the D_o diode is switched off under ZCS conditions. The decreasing rate of the output diode current is controlled by the leakage inductor L_{lk2}, which leads to the improvement of the reverse recovery problem of this diode. Then, after Do turns off and D_3 turns on, L_{m2} is charged via S_2. This interval ends when S_1 is opens.

Mode 4 ($t_3<t<t_4$)

In this state, switch S_1 turns off and diode D_1 starts conducting, while diodes D_2 and D_o are off. The energy of L_{LK1} is transmitted through diodes D_1 to capacitors C_{c2} and C_{c1}, and the S_1 switch voltage is clamped by both capacitors C_{c2} and C_{c1}.

Mode 5 ($t_4<t<t_5$)

This situation begins with diode D_2 turning on as ZCS. When D_4 turns on, the energy stored in capacitor C_{c1} is transferred to the C_L series capacitor. With the secondary current and increase in the voltage of C_L, the voltage across diode D_3 decreases. The energy L_{lk1} is also transferred to the C_{c2} clamp capacitor. Also, the energy of C_{c1} is transferred to the C_L through D_2. The D_o diode is off and the output load energy is supplied through the C_o capacitor, and the inductors L_{m2} and L_{lk2} are receiving energy from the input source. This situation ends when D_1 turns off.

Mode 6 ($t_5<t<t_6$)

When zero L_{lk1} inductor current reaches zero, diode D_1 turns off as ZCS, thus solving the reverse recovery problem of this diode. In this situation, the L_{m1} current passes through the secondary windings, and the C_L capacitor is charged linearly by L_{m1}. Capacitor C_{c1} also continues to transfer its energy through diode D_2 to capacitor C_L and the current D_2 is reduced. The D_o diode is still off and the output load is supplied by the output capacitor.

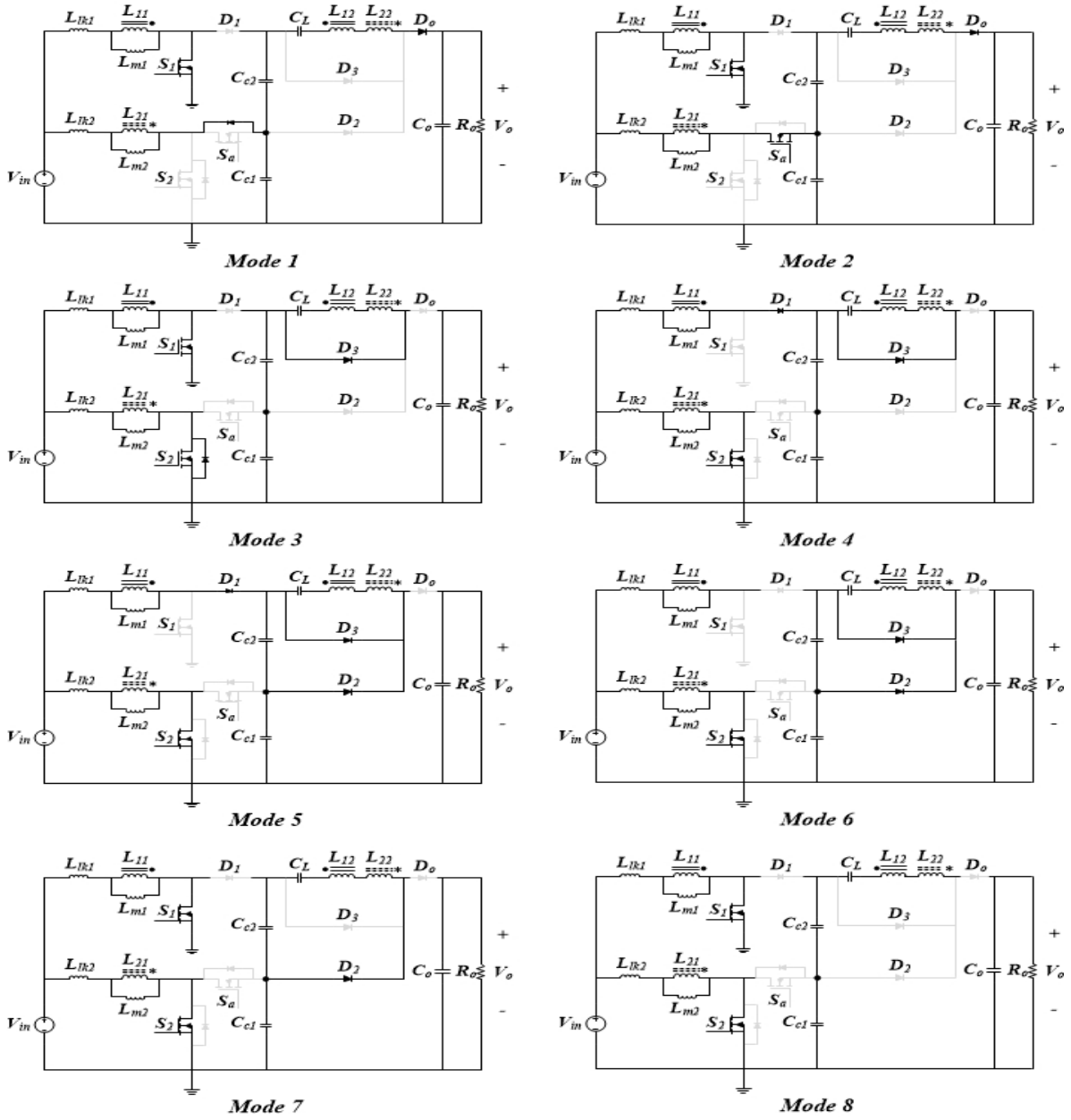

Figure 2. The proposed converter equivalent circuit in the separated eight operation modes

3. PROPOSED CONVERTER DESIGHN CONSIDERATION

3.1. Voltage gain

The voltages of capacitors C_{C1} and C_{C2} are obtained by the volt-second balance relationship of L_{m1} and L_{m2}, respectively.

$$V_{in}DT = (V_{Cc1} - V_{in})(1 - D)T \quad (1)$$

$$V_{Cc1} = \frac{V_{in}}{1-D} \quad (2)$$

$$V_{in}DT = (V_{Cc2} - V_{in})(1 - D)T \quad (3)$$

$$V_{Cc2} = \frac{V_{in}}{1-D} \quad (4)$$

when S_1 is off and D_3 is on, the V_{CL} is obtained by writing KVL in the loop containing the secondary windings and diode D_3.

$$KN(V_{Cc2} - V_{in}) + KNV_{in} - V_{CL} = 0 \quad (5)$$

By inserting the capacitor voltage C_{c2} from Equation (4) in the above equation, the capacitor voltage C_L is obtained as follows:

$$V_{CL} = KN\frac{V_{in}}{1-D} \quad (6)$$

when switch S_1 is off and diode D_1 is on, by writing the KVL relation in the outer loop, the converter voltage gain can be calculated:

$$\frac{V_0}{V_{in}} = \frac{2+2KN+(K-1)D}{1-D} \quad (7)$$

If the coupling factor is considered one, the voltage gain equals to (2+2N)/(1-D) in the ideal state. Figure 3 shows the proposed converter voltage gain versus different duty ratios.

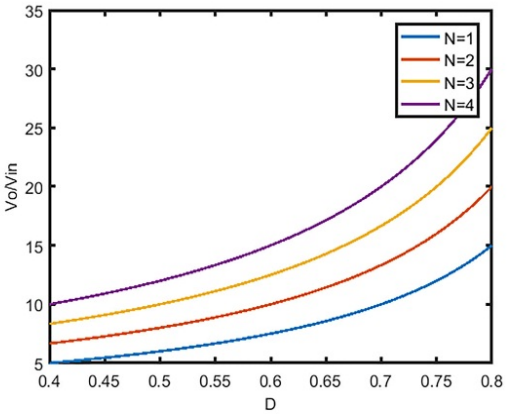

Figure 3. The proposed converter gain versus different duty cycles and turn ratios

3.2. Voltage stress of the semiconductor elements

The voltage of switches S_1 and S_2 is clamped at the voltage level of capacitors C_{c1} and C_{c2}. Therefore, S_1 and S_2 voltage stresses are obtained as follows. The voltage of D_1 is at the level of the total voltage of the clamped capacitors C_{c1} and C_{c2}.

$$V_{S1} = V_{S2} = \frac{V_{in}}{1-D} = \frac{V_0}{2+2KN+(K-1)D} \quad (8)$$

$$V_{D1} = V_{Cc1} + V_{Cc2} = \frac{2V_0}{2+2KN+(K-1)D} \quad (9)$$

when switch S_2 is off, the voltage of D_3 is calculated by writing the following KVL relation.

$$V_{in} - K(V_{C1} - V_{in}) - V_{C1} - V_{D3} + V_0 = 0 \quad (10)$$

By placing the voltage relation of capacitor C_{c2} in the above relation and using the voltage gain relation, the voltage of D_3 is obtained as follows:

$$V_{D3} = \frac{2KN}{2+2KN+(K-1)D}V_0 \quad (11)$$

The voltage stresses of diodes D_2 and D_0 are obtained according to the following equation.

$$V_{D2} = V_{D0} = V_0 - \frac{V_{in}}{1-D} = \frac{1+2KN+(K-1)D}{2+2KN+(K-1)D}V_0 \quad (12)$$

Figure 4 shows the normalized voltage stress of semiconductor elements in terms of output voltage per turn ratios of the windings. As can be seen, upon decreasing the voltage stress of the converter switches with increasing turn ratio (N), the voltage of D_3, D_2, and D_o increases subsequently, which can limit N. However, the stress of the proposed converter diodes is always lower than the output voltage.

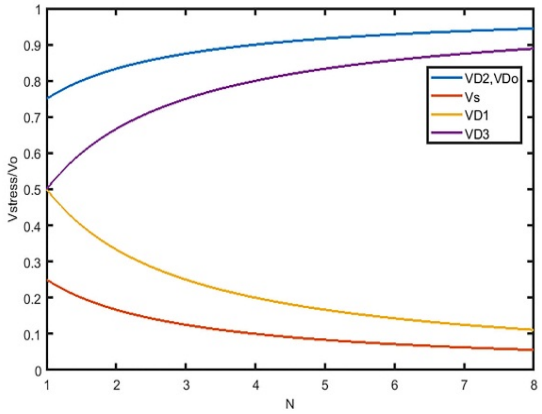

Figure 4. The normalized voltage stress of semiconductor elements in terms of output voltage per turns ratio of the windings

3.3. Design of inductors

To design the inductors, first, the relationship of the magnetizing inductances current is calculated in terms of output current. Then, according to the output power and the amount of inductor current ripple, the values of inductors are obtained. Since the role of capacitor C_{c1} is the voltage clamp of switch S_2 and energy absorption of L_{lk2} and it has a small current, in the calculations, the charge and discharge currents of capacitor C_{c1} as well as diode current D_2 are omitted. Also, the magnetizing inductors are large enough to assume that their current is constant. In addition, the capacitors are designed to be sufficiently large and their voltage can be assumed constant in a steady state. The circumference of the coils of the coupled inductors is considered equal to 2 and the inductors are designed in an ideal state where the coupling coefficient is equal to 1, K =1. When S_1 is turned off, a factor of I_{Lm1}, like AI_{Lm1}, is induced to the secondary. As a result, capacitor C_{c2} is charged with current (1-A) I_{Lm1}. The C_L capacitor is also charged with AI_{Lm1} current, while the S_1 is off. The following equations can be written according to converter operation in turned-on switches.

$$(1-A)I_{Lm1}(1-D)T=\frac{I_{Lm2}}{2}(1-D)T \quad (13)$$

$$I_{Lm2}=2(1-A)I_{Lm1} \quad (14)$$

The current-second balance of capacitor C_{c2} can be written as follows:

$$AI_{Lm1}(1-D)T=\frac{I_{Lm2}}{2}(1-D)T \quad (15)$$

The current-second balance of the C_L capacitor can be written as follows:

$$I_{Lm1}=I_{Lm2} \quad (16)$$

The input current is equal to the sum of the currents of L_{m1} and L_{m2}, and the following relations are accepted for magnetizing currents.

$$I_{in}=I_{Lm1}+I_{Lm2} \quad (17)$$

$$I_{in}=2I_{Lm1} \quad (18)$$

$$I_{Lm1}=I_{Lm2}=\frac{2}{1-D}I_{out} \quad (19)$$

During DT, the inductors L_{m1} and L_{m2} are charged linearly by the input voltage source, V_{in}. Therefore, according to the above relation and considering the current ripple of the inductors, the values of inductors L_{m1} and L_{m2} can be calculated according to the following relation:

$$L_{m1}=L_{m2}=\frac{V_{in}D}{\Delta I_{Lm}f} \quad (20)$$

3.4. Design of capacitors

The capacitors are designed according to current-second balance. Thus, based on the discharge current of capacitors C_1 and C_3 and considering the same discharge energy for these two capacitors, the value of these capacitors can be obtained:

$$\frac{I_{Lm2}}{2}(1-D)T=C\Delta V_C \quad (21)$$

$$C_{c2}=C_L=\frac{I_{out}}{f\Delta V_C} \quad (22)$$

During (1-D) T, the output capacitor C_o is discharged by the I_{out} current in the output. Therefore, the value of C_o can be designed as follows:

$$I_{out}(1-D)T=C_0\Delta V_{C0} \quad (23)$$

$$C_0=\frac{I_{out}(1-D)}{f\Delta V_{Co}} \quad (24)$$

The L_{lk2} energy is absorbed by C_{c1}, which should cause a small voltage ripple in this capacitor.

$$C_{c1}=\frac{L_{lk2}I_{Lm2}^2}{2\Delta V_{Cc1}} \quad (25)$$

4. THE EXPERIMENTAL RESULTS

The prototype of the converter is designed and implemented according to Table 1. The photograph of the implemented converter is shown in Figure 5. The measured voltage and current of switches S_1 and S_2 are shown in Figures 6a and 6b, respectively. In Figure 6a, the current starts to increase with slope and, therefore, zero current switching is established; in addition, the switch voltage has been clamped well. In Figure 6b, the switch current is negative at the turn-on instant, and as a result, its body diode conducts and provides ZV condition. Due to zero voltage switching, the capacitive turn-on losses can be neglected. Figure 6c illustrates the measured drain-source voltage and current of S_a. This switch turns on under ZV condition and all the advantages of S_2 have been established for the auxiliary switch.

Figure 6d shows the current of D_o, and according to this figure, diode turns off under ZC condition. Thus, reverse recovery problem is solved. The practical currents of D_1 and D_2 are given in Figures 6e and 6f, respectively, which indicate that the mentioned diodes do not have a reverse recovery problem.

The proposed converter efficiency has been measured at different loads, as shown in Figure 7. As can be seen from the diagram, the efficiency of the converter is 94 % at full load, which also decreases efficiency with decreasing load, and this is due to constant circuit losses in the clamp circuit. The proposed converter has higher efficiency of 5 % than the hard-switched counterpart. In the hard-switched counterpart, due to the parasitic inductance of coupled inductors, a clamp circuit is required to protect the switches, imposing high losses on the converter.

Table 1. The specification of the proposed interleaved high gain converter

Parameter	Description	Value/Part no.
V_{in}	Input voltage	48 V
V_{out}	Output voltage	480 V
P_{out}	Output power	580 W
f_{sw}	Switching frequency	50 kHz
C_L	Charge-pump capacitor	22 µF
C_{c1},C_{c2}	Clamp capacitor	22 µF
C_o	Output capacitor	47 µF
S_1,S_2	Main switches	IRF740
Sc	Auxiliary switch	IRF740
D_1, D_2,D_3,D_o	Clamp diodes	MUR860

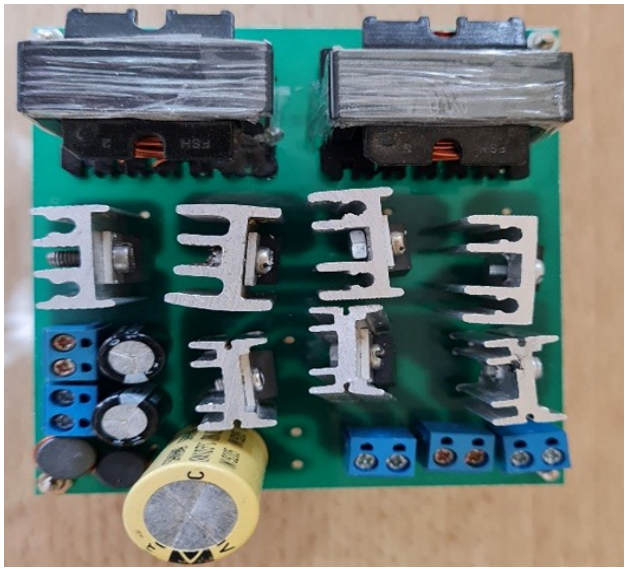

Figure 5. The photograph of the implemented converter

Figure 6. Practical results of the semiconductor elements, a) Measured voltage and current waveforms of S_1 (50 V/div, 10 A/div, 2.5 µs/div), b) Measured voltage and current waveforms of S_2 (50 V/div, 10 A/div, 2.5 µs/div), c) Measured voltage and current waveforms of S_a (50 V/div, 5 A/div, 2.5 µs/div), d) Measured current waveform of D_o (5 A/div, 2.5 µs/div), e) Measured current waveform of D_1 (10 A/div, 2.5 µs/div), f) Measured current waveform of D_2 (2 A/div, 2.5 µs/div)

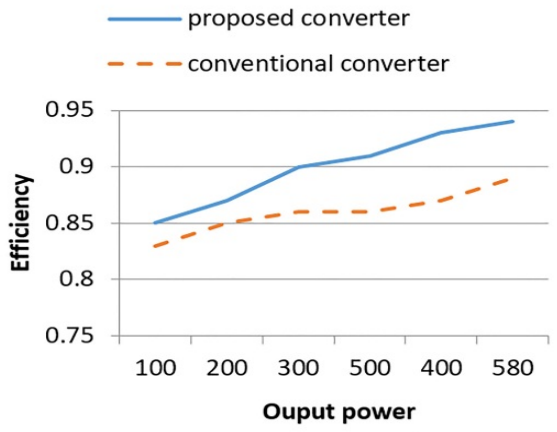

Figure 7. The proposed converter efficiency in comparison with hard-switched counterpart versus different loads

4.2. The comparison between the proposed high step-up converter and the other ones

In this section, the proposed converter is compared with a number of recent high step-up interleaved converters. As can be seen from Table 2, only the converter [26] has fewer elements than the proposed converter. However, the proposed converter has a double voltage gain and the main switch voltage stress is half that of [26].

In terms of voltage gain, converters [14, 28] are in better gain than the proposed converter; however, the converter [14] has four switches that make the operation of the converter more complex and the converter [28] has 24 elements, which increase the conduction loss of the converter and reduce the power density compared to the suggested converter.

Converters [15, 17, 29] operate under ZCS condition and as a result, there are capacitive turn-on losses in these converters. Since the voltage across the switches is high, these losses have a significant role in the total converter losses. Converters [22, 30-31] are hard switching converters. Therefore, in addition to conductive losses, there are switching losses that reduce converter efficiency. Converter [30] has only one switch, which has limited the power of the converter. Likewise, the

hard switching of the power switches has reduced the switching frequency and increased the volume of the converter. According to Table 2, it can be concluded that the proposed converter has a small number of elements and high voltage gain compared to the recent converters, which is highly effective in reducing conduction losses and volume of the converter.

Table 2. The Comparison between the proposed converter and the converters in [14, 15, 17, 21, 25-31]

Parameters / References	Voltage gain	Voltage stress	Switching frequency (kHz)	No. of switches	Total component count	Switching condition
[14]	$\frac{4n}{1-D}$	$\frac{V_{Out}}{4n}$	50	4	17	ZVS
[15]	$\frac{2(1+n)}{1-D}$	$\frac{V_{Out}}{2(1+n)}$	100	2	16	ZCS
[17]	$\frac{2(1+n)}{1-D}$	$\frac{V_{Out}}{2(1+n)}$	100	2	15	ZCS
[21]	$\frac{1+nD}{1-D}$	$\frac{V_{Out}}{1+n}+\frac{n(1-D)}{1+nD}$	25	3	15	Hard
[25]	$\frac{2(1+n)}{1-D}$	$\frac{V_{Out}}{2(1+n)}$	100	2	17	ZVS
[26]	$\frac{(1+n)}{1-D}$	$\frac{V_{Out}}{(1+n)}$	50	4	12	ZVS
[27]	$\frac{2(1+n)}{1-D}$	$\frac{V_{Out}}{2(1+n)}$	100	3	16	ZVS
[28]	$\frac{1+3n}{1-D}$	$\frac{V_{Out}}{1+3n}$	100	3	24	ZVS
[29]	$\frac{2(1+n)}{1-D}$	$\frac{V_{Out}}{2(1+n)}$	118	2	18	ZCS
[30]	$\frac{(4+n(2-D)-D)}{1-D}$	$\frac{V_{Out}}{(4+n(2-D)-D)}$	40	1	18	Hard
[31]	$\frac{(2+n)}{1-D}$	$\frac{V_{Out}}{(2+n)}$	100	2	14	Hard
Proposed converter	$\frac{2(1+n)}{1-D}$	$\frac{V_{Out}}{2(1+n)}$	100	3	13	ZVS-ZCS

5. CONCLUSIONS

In the proposed converter, the combined coupled-inductor structure and the switched capacitor were used to increase the gain. The interleaved technique was employed to reduce total current ripple in the input, which helped achieve the maximum power point of solar cells. To increase the switching frequency and decrease the switching losses, an auxiliary circuit with a minimum number of elements was proposed. The auxiliary switch was also soft switched, so the auxiliary circuit did not impose substantial losses on the converter. On the other hand, the energy of clamp capacitors were transferred to C_L capacitor and then, passed to the output. Therefore, the energy of auxiliary circuit and leakage inductances were not wasted and the clamp capacitors were also effective in increasing the voltage gain. The auxiliary switch was gated in complementary with the S_2 and did not require a separate control algorithm which simplified the implementation of the control circuit. It is recommended that for the future work, the possibility of integrating the auxiliary circuit with the voltage multiplier circuit should be considered to reduce the number of the converter elements and, consequently, decrease the volume and cost of the converter.

6. ACKNOWLEDGEMENT

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NOMENCLATURE

ZVT	Zero voltage transition
ZVS	Zero voltage switching
ZCS	Zero current switching
K	Coupling factor
D	Duty cycle
WCCI	Winding cross coupled inductor
KVL	Kirchoff's voltage law
MOSFET	Metal oxide semiconductor field effect transisitor

REFERENCES

1. Li, W. and He, X., "Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications", ***IEEE Transactions on Industrial Electronics***, Vol. 58, No. 4, (2011), 1239-1250. (https://doi.org/10.1109/TIE.2010.2049715).
2. Fallahzadeh, S., Abjadi, N., Kargar, A. and Blaabjerg, F., "Applying sliding-mode control to a double-stage single-phase grid-connected PV system", ***Journal of Renewable Energy and Environment (JREE)***, Vol. 8, No. 1, (2011), 1-12. (https://doi.org/10.30501/jree.2020.233358.1114).
3. Hassani, M.Y., Maalandish, M. and Hosseini, S.H., "A new single-input multioutput interleaved high step-up DC–DC converter for sustainable energy applications", ***IEEE Transactions on Power Electronics***, Vol. 36, No. 2, (2021), 1544-1552. (https://doi.org/10.1109/TPEL.2020.3011218).

4. Nouri, T., Shaneh, M. and Ghorbani, A., "Interleaved high step-up ZVS DC–DC converter with coupled inductor and built-in transformer for renewable energy systems applications", ***IET Power Electronics***, Vol. 13, No. 16, (2020), 3537-3548. (https://doi.org/10.1049/iet-pel.2020.0162).
5. Li, W., Lv, X., Deng, Y., Liu, J. and He, X., "A review of non-isolated high step-up DC/DC converters in renewable energy applications", ***Proceedings of Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition***, Washington, DC, USA, (2009), 364-369. (https://doi.org/10.1109/APEC.2009.4802683).
6. Esmaeli, A., "An intelligent PV panel structure to extract the maximum power in mismatch irradiance", ***Journal of Renewable Energy and Environment (JREE)***, Vol. 2, No. 1, (2015), 25-31. (https://doi.org/10.30501/jree.2015.70061).
7. Forouzesh, M., Siwakoti, Y.P., Gorji, S.A., Blaabjerg, F. and Lehman, B., "Step-up DC–DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications", ***IEEE Transactions on Power Electronics***, Vol. 32, No. 12, (2017), 9143-9178. (https://doi.org/10.1109/TPEL.2017.2652318).
8. Tofoli, F.L., Pereira, D.D.C. and Paula, W.J., "Survey on non-isolated high-voltage step-up DC–DC topologies based on the boost converter", ***IET Power Electronics***, Vol. 8, No. 10, (2015), 2044-2057. (https://doi.org/10.1049/iet-pel.2014.0605).
9. Kim, P., Lee, S., Park, J. and Choi, S., "High step-up interleaved boost converters using voltage multiplier cells", ***Proceedins of 8th International Conference on Power Electronics - ECCE Asia,*** Jeju, South Korea, (2011), 2844-2851. (https://doi.org/10.1109/ICPE.2011.5944782).
10. Schirone, L. and Macellari, M., "Design of high-efficiency non-insulated step-up converters", ***IET Power Electronics***, Vol. 8, No. 5, (2015), 743-749. (https://doi.org/10.1049/iet-pel.2014.0554).
11. Loera-Palomo, R. and Morales-Saldaña, J.A., "Family of quadratic step-up DC–DC converters based on non-cascading structures", ***IET Power Electronics***, Vol. 8, No. 5, (2015), 793-801. (https://doi.org/10.1049/iet-pel.2013.0879).
12. Zheng, Y., Xie, W. and Smedley, K.M., "Interleaved high step-up converter with coupled inductors", ***IEEE Transactions on Power Electronics***, Vol. 34, No. 7, (2019), 6478-6488. (https://doi.org/10.1109/TPEL.2018.2874189).
13. Yu, W., Hutchens C., Lai, J.S., Zhang, J., Lisi, G., Jabbari, A.D, Smith, D. and Hegardy, T., "High efficiency converter with charge pump and coupled inductor for wide input photovoltaic AC module applications", ***Proceedings of IEEE Energy Conversion Congress and Exposition***, San Jose, CA, USA, (2009), 3895-3900. (https://doi.org/10.1109/ECCE.2009.5316154)
14. Zhu, X., Zhang, B. and Jin, K., "Hybrid nonisolated active quasi-switched DC-DC converter for high step-up voltage conversion applications", ***IEEE Access***, Vol. 8, (2020), 222584-222598. (https://doi.org/10.1109/ACCESS.2020.3043816).
15. Seo, S.-W., Ryu, J.-H., Kim, Y. and Choi, H.H., "Non-isolated high step-up DC/DC converter with coupled inductor and switched capacitor", ***IEEE Access***, Vol. 8, (2020), 217108-217122, (https://doi.org/10.1109/ACCESS.2020.304173).
16. Li, W., Fan, L., Zhao, Y., He, X., Xu, D. and Wu, B., "High-step-up and high-efficiency fuel-cell power-generation system with active-clamp flyback–forward converter", ***IEEE Transactions on Industrial Electronics***, Vol. 59, No. 1, (2012), 599-610. (https://doi.org/10.1109/TIE.2011.2130499).
17. Forouzesh, M., Shen, Y., Yari, K., Siwakoti, Y.P. and Blaabjerg, F., "High-efficiency high step-up DC–DC converter with dual coupled inductors for grid-connected photovoltaic systems", ***IEEE Transactions on Power Electronics***, Vol. 33, No. 7, (2018), 5967-5982. (https://doi.org/10.1109/TPEL.2017.2746750).
18. Li, W.; Li, W. and He, X., "Zero-voltage transition interleaved high step-up converter with built-in transformer", ***IET Power Electronics***, Vol. 4, No. 5, (2011), 523-531. (https://doi.org/10.1049/iet-pel.2010.0133).
19. Nouri, T., Hosseini, S.H., Babaei, E. and Ebrahimi, J., "Interleaved high step-up DC–DC converter based on three-winding high-frequency coupled inductor and voltage multiplier cell", ***IET Power Electronics***, Vol. 8, No. 2, (2015), 175-189. (https://doi.org/10.1049/iet-pel.2014.0165).
20. Li, W., Xiang, X., Li, C., Li, W. and He, X., "Interleaved high step-up ZVT converter with built-in transformer voltage doubler cell for distributed PV generation system", ***IEEE Transactions on Power Electronics***, Vol. 28, No. 1, (2013), 300-313. (https://doi.org/10.1109/TPEL.2012.2199771).
21. Dwari, S. and Parsa, L., "An efficient high-step-up interleaved DC–DC converter with a common active clamp", ***IEEE Transactions on Power Electronics***, Vol. 26, No. 1, (2011), 66-78. (https://doi.org/10.1109/TPEL.2010.2051816).
22. Delshad, M., Madiseh, N.A., Amini, M.R., and Yazdani, M.R., "Implementation of soft-switching bidirectional flyback converter without auxiliary switch", ***IET Power Electronics***, Vol. 6, No. 9, (2013), 1884-1891. (https://doi.org/10.1049/iet-pel.2012.0472).
23. Shamsi, T., Delshad, M. and Adib, E., "A new simple-structure passive lossless snubber for DC-DC boost converters", ***IEEE Transactions on Industrial Electronics***, Vol. 68, No. 3, (2021), 2207-2214. (https://doi.org/10.1109/TIE.2020.2973906).
24. Gerami, E., Delshad, M., Amini, M.R. and Yazdani, M.R., "A new family of non-isolated PWM DC-DC converter with soft switching", ***IET Power Electronics***, Vol. 12, No. 2, (2019), 237-244. (https://doi.org/10.1049/iet-pel.2018.5351).
25. Li, W., Xiang, X., Li, C., Li, W. and He, X., "Interleaved high step-up ZVT converter with built-in transformer voltage doubler cell for distributed PV generation system", ***IEEE Transactions on Power Electronics***, Vol. 28, No. 1, (2013), 300-313. (https://doi.org/10.1109/TPEL.2012.2199771).
26. Li, W. and He, X., "ZVT interleaved boost converters for high-efficiency, high step-up DC-DC conversion", ***IET Electric Power Applications***, Vol. 1, No. 2, (2007), 284-290. (https://digital-library.theiet.org/content/journals/10.1049/iet-epa_20060239).
27. Akhlaghi, B., Molavi, N., Fekri, M. and Farzanehfard, H., "High step-up interleaved ZVT converter with low voltage stress and automatic current sharing", ***IEEE Transactions on Industrial Electronics***, Vol. 65, No. 1, (2018), 291-299. (https://doi.org/10.1109/TIE.2017.2723861).
28. Packnezhad, M., Farzanehfard, H. and Adib, E., "Integrated soft switching cell and clamp circuit for interleaved high-step-up converters," ***IET Power Electronics***, Vol. 12, No. 3, (2019), 430-437. (https://doi.org/10.1049/iet-pel.2018.5446).
29. Alghaythi, M.L., O'Connell, R.M., Islam, N.E., Khan, M.M.S. and Guerrero J.M., "A high step-up interleaved DC-DC converter with voltage multiplier and coupled inductors for renewable energy systems", ***IEEE Access***, Vol. 8, (2020), 123165-123174. (https://doi.org/10.1109/ACCESS.2020.3007137).
30. Andrade, A.M.S., Schuch, S.L. and da Silva Martins, M. L., "Analysis and design of high-efficiency hybrid high step-up DC–DC converter for distributed PV generation systems", ***IEEE Transactions on Industrial Electronics***, Vol. 66, No. 5, (2019), 3860-3868. (https://doi.org/10.1109/TIE.2018.2840496).
31. Zheng, Y., Brown, B., Xie, W. and Li, S., "High step-up DC–DC converter with zero voltage switching and low input current ripple", ***IEEE Transactions on Power Electronics***, Vol. 35, No. 9, (2020), 9416-9429.(https://doi.org/10.1109/TPEL.2020.2968613).