JREE: Vol. 13, No. 1, (Winter 2026) 44-57

Journal of Renewable Energy and Environment

Journal Homepage: www.jree.ir

Materials and Energy Research Center

MERC

Research Article

Enhanced High-Gain Y-Source DC-DC Converter with Switched-Inductor-Capacitor Design for Improved Efficiency and Reliability in Grid-Integrated Solar Power Systems

Nithya Devi S M[a], Vijayakumar K[a], Divya Navamani J[a*], Irfan Ahmad Khan[b*], Pradeep Vishnuram[a], Mohit Bajaj[c,d,e]

[a]Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology, Kattankulathur, Chennai, India.
[b]Department of Electronics and Communication Engineering, Chandigarh College of Engineering and Technology (Degree Wing), Chandigarh, India.
[c]Department of Electrical Engineering, Graphic Era (Deemed to be University), Dehradun, India.
[d]College of Engineering, University of Business and Technology, Jeddah, Saudi Arabia.
[e]Department of Electrical Engineering, Graphic Era Hill University, Dehradun, India.

PAPER INFO

Paper history:
Received: 20 January 2025
Revised: 17 June 2025
Accepted: 22 September 2025

Keywords:
High-Gain Dc-Dc Converter,
Y-Source Network,
Switched Inductor-Capacitor,
Photovoltaic Systems,
Grid-Connected Applications,
Voltage Amplification,
Reliability Analysis,
Energy Efficiency

ABSTRACT

Efficient and reliable high-gain DC–DC converters are critical in photovoltaic (PV) grid-connected systems to bridge the gap between low-output PV voltages and the high input voltages required by the grid. This paper presents a novel high-gain DC–DC converter that integrates a Y-source network with a hybrid switched-inductor-capacitor (SLC) boost module, achieving superior voltage amplification at reduced duty cycles. The proposed converter architecture can achieve a voltage gain of up to 16 times the input voltage with only an 18% duty cycle, thereby minimizing conduction and switching losses and extending the converter's operational lifespan.The design enables continuous current draw from the source while maintaining reduced stress on components, distinguishing it from conventional converters. A detailed steady-state analysis and design methodology for the inductive and capacitive elements are provided, with final component values optimized for performance and reliability. MATLAB/Simulink simulations validate the theoretical analysis, demonstrating an efficiency of 88.8% at 100 W output power and a mean time to failure (MTTF) of 104.14 kHr, representing substantial improvements over existing topologies.Experimental validation on a 100 W prototype confirms the converter's reliability and performance, achieving a stable output voltage of 192 V from a 12 V input. Comparative analysis with traditional Y-source and SLC-based converters highlights the proposed topology's advantages in efficiency, voltage gain, and reduced component count, making it a promising candidate for PV grid applications.

https://doi.org/10.30501/jree.2025.493144.2191

1. INTRODUCTION

Renewable energy sources, including solar, wind, fuel cells, biomass, and tidal energy, are increasingly recognized as essential components of the future energy sector. Their importance stems from their widespread availability, sustainability, and minimal environmental impact. Unlike conventional fossil fuels, which are finite and environmentally detrimental, renewable energy sources provide a cleaner and more sustainable pathway to meet the growing global energy demand driven by population growth and industrial expansion (G.Buticchi et al.,2021). As societies worldwide seek to decarbonize energy systems and address climate change, these renewable sources are poised to play a central role in reshaping the energy landscape.

However, efficiently harnessing energy from these sources presents significant challenges due to their intermittent nature. Variability in sunlight, wind speed, and other environmental factors causes fluctuations in energy output, leading to inconsistencies in power generation. For example, solar power generation varies substantially between day and night and under cloudy conditions, while wind energy depends heavily on local wind patterns. This intermittency complicates direct integration of renewable energy sources into the grid, as the generated energy is often unregulated and inherently unstable, producing a low and fluctuating DC voltage at the output. Consequently, there is a critical need for power electronic converters capable of converting and regulating this unstable DC voltage to match the grid's stable AC or DC voltage levels. Significant research has therefore focused on developing power electronic converters that are efficient, reliable, and capable of providing high voltage gain. Such converters are essential for integrating renewable energy into the power grid, as they boost the low and variable DC output of renewable sources to a high, stable DC or AC level suitable for grid-connected applications (Y.Yang et al.,2015).Cost-effectiveness is another crucial factor, as affordable converter solutions enable broader adoption of renewable technologies and support the development of sustainable energy systems globally (Anitha.P et al.,2003).The development of high-gain, efficient, and reliable DC–DC converters is thus central to advancing

*Corresponding Author's Email: divyanaj@srmist.edu.in (D. Navamani J) irfan00706@gmail.com (I. Ahmad Khan)
URL: https://www.jree.ir/article_230066.html

Please cite this article as: Devi, S. M. N., Vijayakumar, K. A., Navamani, J. D., Khan, I. A., Vishnuram, P., & Bajaj, M. (2025). Enhanced High-Gain Y-Source DC-DC Converter with Switched-Inductor-Capacitor Design for Improved Efficiency and Reliability in Grid-Integrated Solar Power Systems. *Journal of Renewable Energy and Environment (JREE)*, *13*(1), 44-57. https://doi.org/10.30501/jree.2025.493144.2191.

renewable energy technologies, with extensive research dedicated to optimizing these devices for renewable energy applications.

Figure 1 illustrates the essential role of DC–DC converters in renewable energy power generation, highlighting their contribution to stable and high-quality power integration into the electrical grid (A.Chub et al.,2015).

Initially, conventional topologies such as boost converters, multilevel converters, cascaded converters, and voltage multiplier cells were employed to enhance output voltage and improve voltage gain (F.M.Shahir et al.,2019). However, these approaches suffer from several limitations.

- They operate at high duty cycles, resulting in significant conduction and switching losses.
- At duty cycles above 50%, inductor current saturation increases, reducing converter performance (M.Forouzesh et al., 2017).
- A high component count increases the converter's weight, complexity, and cost.
- System reliability is compromised, as the failure of a single component may damage the overall system.
- Voltage gain remains relatively low.
- These converters draw discontinuous current from the source, which decreases lifetime and introduces harmonics into the system

Therefore, it is essential to develop a power electronic converter with the following characteristics:

- A high voltage transfer ratio
- Low conduction and switching losses
- High reliability
- Continuous current draw from the source
- Minimal component count

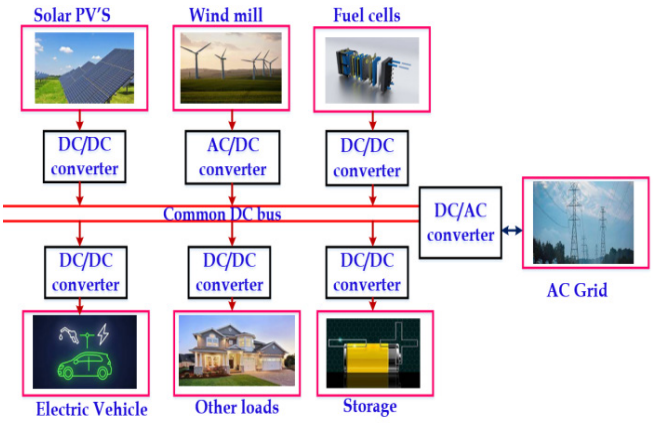


Figure 1. The layout of DC-DC converters with renewable energy application

Over the years, several DC–DC converter topologies have been developed to meet these requirements (M.Forouzesh et al., 2017). Among them, coupled inductor topologies and impedance source networks have received considerable attention due to their inherent boost capability, extended voltage range, and ability to draw continuous input current. Importantly, these topologies can achieve high voltage gain at lower duty cycles compared to conventional DC–DC converters (Liu H.Ji, et al, 2018). Figure 2 illustrates the key applications of impedance source networks. The impedance source networks were first introduced by F.Z. Peng in the year 2003 (Fang Zheng Peng, 2003). Despite the numerous advantages, their performance is affected by the parasitic effect of inductance in the impedance network (BabayiNozadian, Mohsen,et al.,2019).

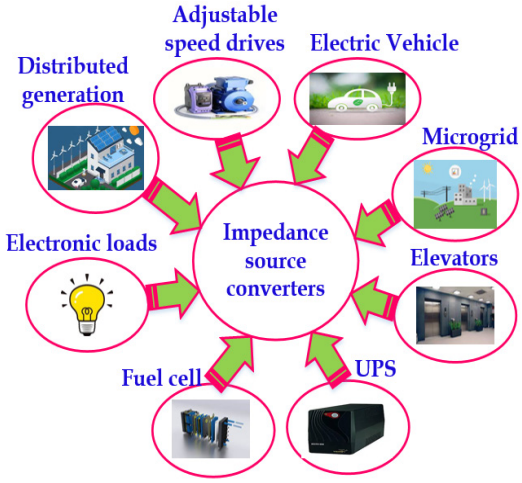


Figure 2. Applications of impedance source converters

Ever since their inception, numerous modifications have been made to the conventional Z source network to improve their overall performance (Y. P. Siwakoti et al,2015). Z source networks were followed by quasi Z source(Liu, H.,Ji et al,2018), switched Z source(BabayiNozadian et al,2019), hybrid Z source(D. Cao et al,2009) (Shen, H et al,2017), LCCT Z source (Adamowicz,M et al,2011), T source (Strzelecki,R et al, 2009), a source (Siwakoti, Y et al, 2016),€ source(Soon, J. J et al., 2014), Δ source, Γ source (Loh, P. C et al., 2013), Y source (Siwakoti, Y. P et al., 2014), etc. Among the newly derived topologies, Y source networks are identified to be relevant and promising because of their high voltage gain at lower duty ratios compared to the traditional ones.

Y-source networks were first introduced by Yam Siwakoti in 2014 (Siwakoti, Y. P et al., 2014). Figure 3(a) shows the traditional Y-source converter, a single-switch topology consisting of a three-winding coupled inductor, an input diode, and a switch. The voltage gain of this converter is expressed as G_v=1/1-K_dD, where D is the duty ratio and K_d is the winding factor. The converter's gain depends on both the duty cycle and the winding factor, and theoretically, it can achieve a maximum voltage gain up to ten times the input voltage. Despite its high voltage gain, the conventional Y-source converter exhibits several drawbacks. The input D_{in} draws discontinuous current during each biasing state, and the switch experiences a high inrush current at startup.

In the study of Wang et al. (2019),a switched-inductor boost module was added to the input to enhance converter performance, as shown in Figure 3(d) (Yuan,J.et al.,2020). This modification ensures continuous source current; however, the voltage gain is limited to six times the input voltage at a duty cycle of 18% and a winding factor of 3. To further improve the voltage gain at a lower duty cycle, the switched-inductor boost module was replaced with a switched-inductor–capacitor (SLC) boost module. Specifically, the diode D_2 in Figure 3(d) was replaced with a capacitor C in Figure 3(e). This simple modification increases the converter's voltage gain to 16 times the input voltage while maintaining the same duty cycle and winding factor.

In the study of Wang et al. (2019),a switched-inductor boost module was added to the input to enhance converter performance, as shown in Figure 3(d) (Yuan,J.et al.,2020). This modification ensures continuous source current; however, the voltage gain is limited to six times the input voltage at a duty

cycle of 18% and a winding factor of 3. To further improve the voltage gain at a lower duty cycle, the switched-inductor boost module was replaced with a switched-inductor–capacitor (SLC) boost module. Specifically, the diode D_2 in Figure 3(d) was replaced with a capacitor C in Figure 3(e). This simple modification increases the converter's voltage gain to 16 times the input voltage while maintaining the same duty cycle and winding factor.

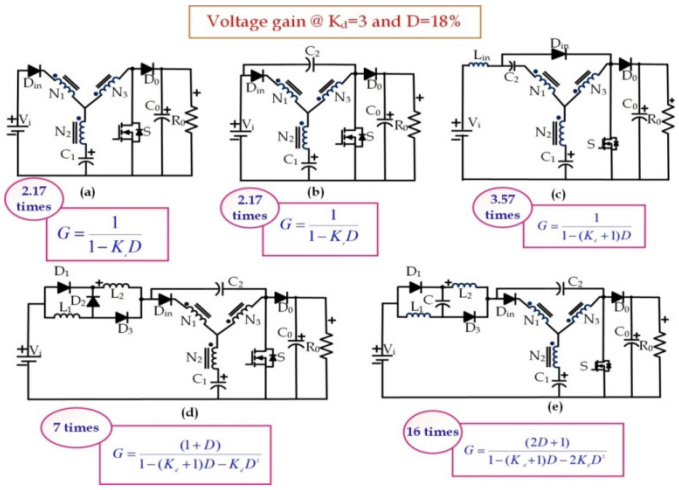


Figure 3. (a).Y-Source-DC/DC converter (Siwakoti, Y. P et al., 2014); (b). Improved Y-source converter (Siwakoti, Y. P et al., 2015); (c). Quasi Y-source converter (Yuan,J.et al.,2020)) (d)SLY source converter (Wang et al. (2019)); (e) Proposed topology

While the topologies shown in Figures 3(c) and 3(d) achieve a maximum gain of only 7 times the input voltage, the proposed topology attains a gain of 16 times, as discussed in subsequent sections. This study introduces a novel converter topology that combines a Y-source network with an SLC boost module. The proposed design delivers significantly enhanced voltage gain, improved reliability, and continuous input current, making it highly suitable for efficient PV integration at reduced duty cycles.

An in-depth design and steady-state analysis of the converter is presented, supported by MATLAB/Simulink simulations and experimental validation on a 100 W prototype. Comparative analysis with conventional converters further demonstrates the advantages of the proposed topology, particularly in terms of efficiency, reduced component stress, and reliability, making it a promising solution for modern PV applications.

The remainder of this paper is organized as follows: Section II provides a detailed analysis and discussion of the proposed converter's operating principles, including circuit configuration, operating modes, and the design of the SLC module. Section III presents the steady-state analysis, deriving key equations for voltage transfer, current characteristics, and voltage gain. Section IV examines boundary conditions to establish operational limits under continuous conduction mode, while Section V details current calculations across each converter component. Section VI addresses voltage and current stress calculations to evaluate component reliability under operating conditions. Section VII discusses the design considerations for inductors and capacitors to ensure optimal component selection and enhanced performance. Section VIII analyzes converter efficiency by quantifying power losses in diodes, inductors, and switches. Section IX presents reliability analysis, focusing on the Mean Time to Failure (MTTF) using military-standard specifications. Section X compares the proposed converter's performance with existing literature, emphasizing voltage gain, component count, and reliability. Section XI showcases simulation and experimental results to validate performance, and Section XII concludes the paper, summarizing the main findings and potential directions for future research.

2. ANALYSIS AND WORKING OF THE PROPOSED CONVERTER

2.1 Circuit configuration

Figure 4 illustrates the proposed topology. A switched-inductor–capacitor (SLC) cell is incorporated between the input and the coupled inductor. The boost cell consists of two diodes, one capacitor, and two inductors. Adjacent to the boost module is the improved Y-source converter cell, which comprises a three-winding coupled inductor arranged in a Y configuration with turns N_1, N_2, and N_3. Capacitor C_2 is connected to suppress inrush current, and the switch SSS is placed next to the three-winding inductor. The load is connected downstream of the semiconductor switch with a capacitor C_0 and an isolation diode D_0.The SLC module at the input enhances the voltage gain and ensures continuous source current. Key features of the proposed converter include:

- A voltage transfer ratio of up to 16 times the input voltage at a duty cycle D=18%.
- Suppression of inrush current at startup and continuous source current.
- High efficiency of 88.8%.
- Robust reliability, with an MTTF of 104.14 kHr.

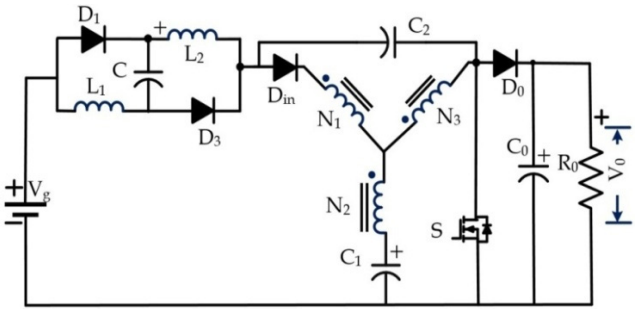


Figure 4. Proposed topology

2.2 Principal of operation

Assumptions**:**

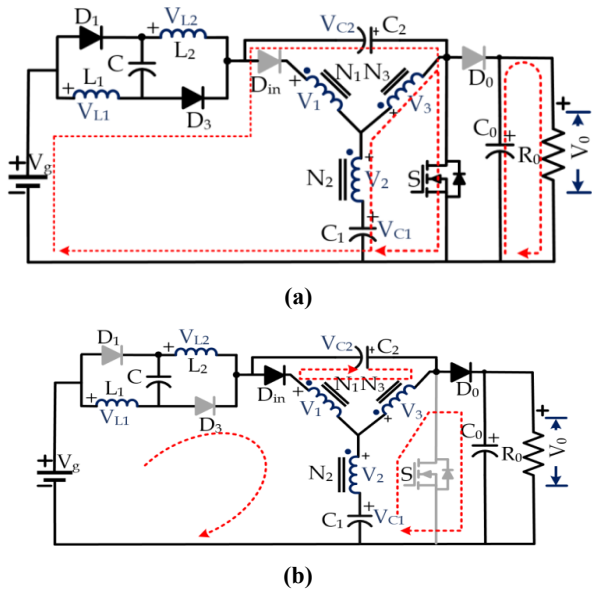
- All the components are assumed ideal.
- The converter operates in steady state.
- Leakage inductances are neglected.
- A constant voltage is maintained across the capacitors.

The voltages across the inductors L_1 and $L_2$are V_{L1} and V_{L2}, respectively. The source voltage is given as V_g. The voltages across the capacitors C_1 and C_2 are V_{C1} and V_{C2}, respectively. The load voltage is V_0. The number of turns in the winding is N_1, N_2, and N_3, respectively. The voltages across the turns N_1, N_2 and N_3 are V_1, V_2, and V_3,respectively. The switch voltage is V_{sw}. The voltage across the capacitor 'C' in the boost module is V_C. Similarly, the currents through the inductors L_1 and $L_2$are I_{L1} and I_{L2}, respectively. The source current is given as I_{in}. The currents through the capacitors C_1 and C_2 are I_{C1} and I_{C2} respectively. The load current is I_0. The currents through the turns N_1, N_2, and N3 are I_1, I_2, and I_3, respectively. The switch current is I_{sw}. The current through the capacitor 'C' in the boost module is I_C.The currents through the diodes D_1 and D_2 are I_{D1} and I_{D2}, respectively. The winding factor of the three-winding

coupled inductor is k_d. Voltage equations are derived using Kirchhoff's Voltage Law (KVL), and current equations are obtained using Kirchhoff's Current Law (KCL). The duty cycle at which the switch operates is denoted by'D'.

2.3 Mode 1[to = 0<t<t1 = DTs]

Figure 5(a) depicts the shoot-through (turn-on) operation of the converter.



(a)

(b)

Figure 5. (a). Mode 1. [$t_o = 0<t<t_1 = DT_s$];(b). Mode 2. [$t_1 = (1-D)T_s<t<t_2 = T_s$]

The switch is activated by a gate pulse fromt_0 to $t_1(0\text{-}DT_s)$. During this interval, the input diodeD_{in} bbetween the boost module and the coupled inductor is reverse-biased. Capacitor C_1begins charging the secondary winding N_2 of the coupled inductor. The output capacitor C_0begins energizing the load. The diodes in the SLC module (D_1, D_2) start charging the inductors in SLC module (L_1, L_2). The currents through the inductors start increasing linearly during this time. Considering the symmetrical configuration of the switched-inductor–capacitor module and assuming the inductors in the boost module have identical values, the current rise is uniform across both inductors.

$V_{L1} = V_{L2} = V_L$.

Applying Kirchhoff's Voltage Law (KVL), the voltage equations for the converter are expressed as Eq. (1)-(4):

$$V_L = V_g + V_{C2} \quad (1)$$

$$V_{C1} + V_2 - V_3 = 0 \quad (2)$$

$$V_{C1} + V_2 = V_3 \quad (3)$$

Since $\frac{V_1}{V_2} = n_{12}$ and $\frac{V_3}{V_2} = n_{32}$,

$$V_2 = \frac{V_{C1}}{n_{32}-1} \quad (4)$$

Where $n_{12} = \frac{N_1}{N_2}$ and $n_{32} = \frac{N_3}{N_2}$ are the turn's ratios.

The current equations are presented in Eq. (5)-(10)

$$I_{L1} = I_{in} - I_C - I_{L2} \quad (5)$$

$$I_{L2} = I_{in} - I_C - I_{L1} \quad (6)$$

$$I_C = I_{in} - I_{L1} - I_{L2} \quad (7)$$

$$I_{C2} = I_{L1} + I_C + I_{L2} \quad (8)$$

$$I_{SW} = I_3 + I_{C2} \quad (9)$$

$$I_{D1} = I_{L1}; I_{D2} = I_{L2} \quad (10)$$

2.4 Mode 2[t1 = (1-D)Ts<t<t2 = Ts]

Figure 5(b) illustrates Mode 2 operation of the converter. At the time instant DT_s (t_1), the switch turns off, and the diodes in the SLC module (D_1 and D_2) become reverse-biased. During this interval, the switch voltage V_{SW} rises. The capacitors associated with the boost network (C), the secondary winding (C_1), and the coupled inductors (C_2) undergo recharging. Simultaneously, the inductorsL_1 andL_2 begin releasing their stored energy, causing the inductor currents to decrease until the switch is turned on again at t_2.

Upon applying KVL to the circuit, the voltage equations are given from Eq. (11)-(14)

$$V_g - V_{L1} - V_C - V_{L2} - V_1 - V_2 - V_{C1} = 0 \quad (11)$$

Assuming

$$V_{L1} = V_{L2} = V_C$$

$$V_g - 3V_{L1} - V_1 - V_2 - V_{C1} = 0$$

$$V_L = [V_g - V_1 - V_2 - V_{C1}]/3 \quad (12)$$

$$V_1 + V_3 + V_{C2} = 0 \quad (13)$$

$$n_{12}\overline{V_2} + n_{32}\overline{V_2} + V_{C2} = 0$$

Where

$$\overline{V_2} = \frac{-V_{C2}}{n_{12}+n_{32}} \quad (14)$$

The current equations are given from Eq. (15)-(19)

$$I_{L1} = I_{L2} = I_C = I_{in} \quad (15)$$

$$I_2 = I_{C2} \quad (16)$$

$$I_1 = I_{in} - I_{C2} \quad (17)$$

$$I_3 = I_1 + I_2 \quad (18)$$

$$I_{D1} = I_{L1}; I_{D2} = I_{L2} \quad (19)$$

3. STEADY STATE ANALYSIS

Figure 6 shows the equivalent circuit of the proposed converter, while Figures 7(a), 7(b), and 7(c) illustrate the current and voltage waveforms of the individual components.

Applying volt second balance principle to V_L (1) and (12) $DV_L + (1-D)\overline{V_L} = 0$, the inductor voltage in Mode 2(off state) is

$$\overline{V_L} = V_g - V_1 - V_2 - V_{C1}$$

$$V_1 = n_{12}V_2$$

$$\overline{V_L} = [V_g - (1+n_{12})\overline{V_2} - V_{C1}]/3$$

Substituting (8) and (21) in (20), we have:

$$D(V_g + V_{C2}) + (1-D)[(V_g - (1+n_{12})\overline{V_2} - V_{C1})/3] \quad (20)$$

Applying volt second balance principle to V_2(4) and (14), we have:

$$DV_2 + (1-D)\overline{V_2} = 0, D(\frac{V_{C1}}{n_{32}-1}) + (1-D)(\frac{-V_{C2}}{n_{32}+n_{12}}) = 0 \quad (21)$$

The voltage across Capacitors C_1 and C_2 is calculated by solving (20) and (21) and is given in (22)-(24):

$$V_{C1} = \frac{(1+2D)V_g(1-D)V_g}{1-D(K_d+1)-2K_dD^2} \quad (22)$$

$$V_{C2} = \frac{(1+2D)K_d D V_g}{1-(K_d+1)D-2K_d D^2} \quad (23)$$

The voltage across the inductor is

$$V_L = \frac{(D+2K_d D+1))V_g}{1-(K_d+1)D-2K_d D^2} \quad (24)$$

The winding factor K_d of the converter is calculated as:

$$K_d = \frac{n_{12}+n_{32}}{n_{32}-1}$$

The peak output voltage in the turn off state is calculated as

$$\overline{V_0} = V_{C1} + \overline{V_2} - \overline{V_3}$$

$$= V_{C1} + \overline{V_2}(1-n_{32})$$

$$= V_{C1} + V_{C2}/K_d$$

The output voltage and the corresponding transfer function are calculated and presented in equations (25) and (26)

$$V_0 = \frac{(2D+1)V_g}{1-(K_d+1)D-2K_d D^2} \quad (25)$$

The voltage gain of the switched inductor-capacitor Y-source converter is as follows:

$$\frac{V_0}{V_g} = \frac{(2D+1)}{1-(K_d+1)D-2K_d D^2} \quad (26)$$

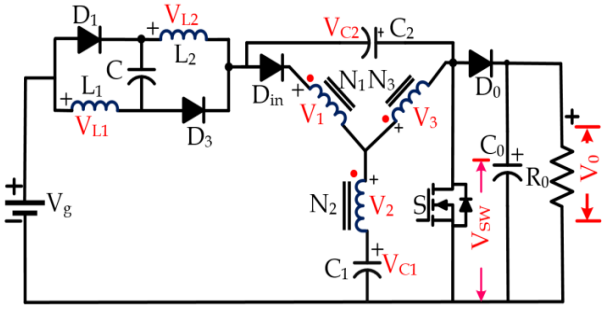


Figure 6. Equivalent circuit of the converter

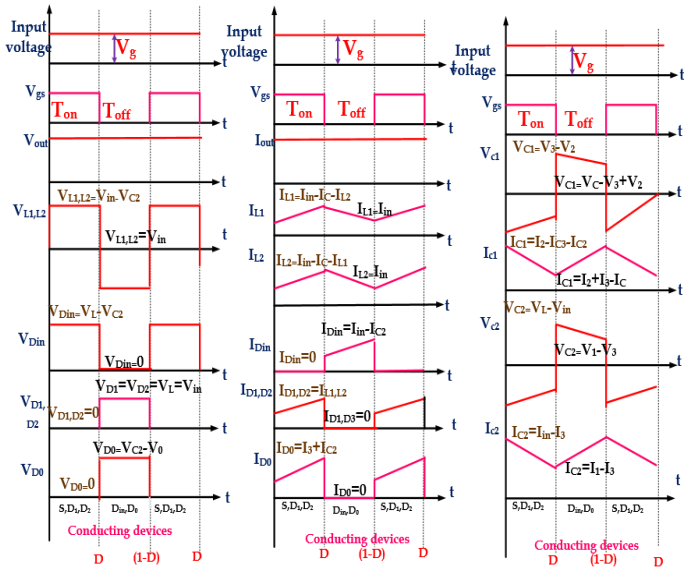


Figure 7. (a) & (b) Voltage and current waveforms of inductors and diodes (c) Voltage and current waveform of capacitors

Figure 8 presents a comparison of the voltage gain of existing Y-source-based converters at a duty cycle of 18% and a winding factor K_d=3. The figure clearly demonstrates that the proposed topology achieves a higher voltage gain than the existing topologies.

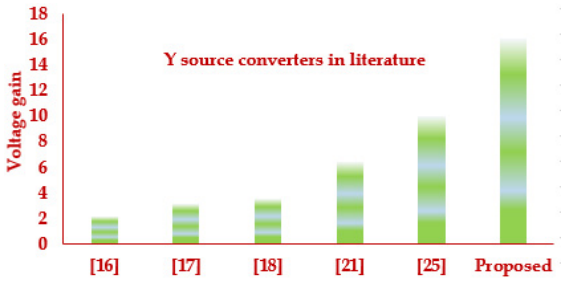


Figure 8. Comparison of the voltage gain of Y source SLC with different converters at duty ratio d=0.18 and turns ratio K_d=3

The voltage gain equation derived in (26) was used to generate Table 1. This equation indicates that the voltage gain depends on both the duty cycle and the winding factor. Table 1 presents the voltage gain of the proposed topology for different turn ratios and duty cycles. Each row corresponds to the voltage gain for a specific winding factor, while the fourth column shows various combinations of turn ratios for that winding factor. It is observed that, for a given duty cycle and winding factor, the voltage gain remains constant regardless of the specific turn ratio combinations. However, the voltage gain can be adjusted by changing the turn ratios, highlighting the versatility of the converter, as its gain can be controlled through both internal and external parameters.

Table 1. Voltage gain of SLC Y-source with different K and winding turns ratio

K_d	Gain	Range of D	Possible combinations of $N_1/N_2/N_3$	Example
2	$G_v=\frac{(2D+1)}{1-3D-4D^2}$	0 < D <0.3	(1,1,3);(1,2,5);(1,3,7);(1,4,9);(2,1,4);(2,3,8);(3,1,5);(4,1,6)	D=0.15, G=2.54; D=0.2, G=5.833
3	$G_v=\frac{(2D+1)}{1-4D-6D^2}$	0 <D < 0.25	(1,1,2);(1,3,5);(1,5,8);(2,4,7);(3,1,3);(3,5,9);(4,2,5) 4:6:11	D=0.15, G=3.90 D=0.18, G=16
4	$G_v=\frac{(2D+1)}{1-5D-8D^2}$	0 <D < 0.20	(1,2,3);(1,5,7);(2,1,2);(3,3,5);(4,5,8)(5,1,3);(5,4,7);(8,1,4)	D=0.1, G=2.60 D=0.12, G=3.62
5	$G_v=\frac{(2D+1)}{1-6D-10D^2}$	0 <D <0.15	(1,3,4);(2,2,3);(3,1,2);(3,5,7);(5,3,5);(7,1,3);(8,4,7)	D=0.1, G=3.42 D=0.12, G=5.96

Figure 9 illustrates the effect of the winding factor on the voltage gain of the converter. It is evident that increasing the winding factor leads to a corresponding increase in voltage gain.

Figure 9. Voltage gains with different duty ratios and winding factor

4. BOUNDARY CONDITION OF THE CONVERTER

The voltage transfer ratio is determined by assuming that the converter operates in continuous conduction mode (CCM). The critical inductance (L_{crit}) is calculated at the boundary between CCM and discontinuous conduction mode, representing the maximum inductance value for which the converter can maintain continuous conduction. The inductor currents are equal, $I_{L1}=I_{L2}=I_L$, and the current change during the turn-on and turn-off periods is denoted as ΔI_L. The converter operates at a switching frequency f_s. Equations (27)-(29) provide the expressions for the inductor current variation and the critical inductance value.

$$I_L \geq \Delta I_L \tag{27}$$

$$I_L = \frac{V_0^2}{V_i R_0}\left[\frac{1}{(4-D)}\right],\ \Delta I_L = \frac{V_i(K_d D+D+1)}{1-(K_d+1)D-2K_d D^2} * \frac{DT}{L} \tag{28}$$

Solving (27) and (28)

$$\frac{f_s L}{R_0} \geq \frac{D(4-D)(K_d D+D+1)}{1-(K_d+1)D-2K_d D^2} * \frac{DT}{L}$$

Where $K_{cric(L)} = \frac{f_s L}{R_0}$

$$K_{cric(L)} = \frac{D(4-D)(K_d D+D+1)}{1-(K_d+1)D-2K_d D^2} * \frac{DT}{L} \tag{29}$$

5. CURRENT CALCULATIONS

By applying the ampere–second balance principle and solving equations (5)–(10) and (15)–(19), the currents through the various components of the converter are derived. Equations (30)–(40) present these component current expressions.

The capacitor (C_1) current

$$IC1=I_{in}+(1-D)I_0 \tag{30}$$

The capacitor (C_2) current

$$Ic2=\frac{(N_2-N_3)(I_{in}-I_0)}{(N_1-N_3)} \tag{31}$$

The inductor current,

$$IL=\frac{V_0^2}{V_g R_0}\left(\frac{1}{4-D}\right) \tag{32}$$

The average value of diode (D_{in}) current,

$$IDin(avg)=\frac{(1-D)I_0}{K_d D} \tag{33}$$

The rms value of diode (D_{in}) current,

$$IDin(rms)=\frac{K_d(1-D)I_0}{\sqrt{1-D}} \tag{34}$$

The rms value of diode ($D_{1,2}$) current,

$$ID1=ID2(rms)=\frac{K_d I_0}{\sqrt{D}} \tag{35}$$

The average value of diode ($D_{1,2}$) current,

$$I_{D1}=I_{D2(avg)}=\frac{K_d I_0}{D} \tag{36}$$

The average value of diode (D_0) current,

$$I_{Do(avg)}=I_0 \tag{37}$$

The rms value of diode (D_0) current,

$$IDo(rms)=\frac{I_0}{\sqrt{D}} \tag{38}$$

The rms value of switch current,

$$ISW(rms)=\frac{I_0}{\sqrt{1-D}} \tag{39}$$

The average value of switch current,

$$ISW(peak)=\frac{I_0(1-D)}{\sqrt{D}} \tag{40}$$

6. VOLTAGE AND CURRENT STRESS CALCULATIONS

When the switch is in off state, the voltage across the switch is equal to the load voltage. The switch voltage stress is obtained in (41)

$$\frac{V_{SW}}{V_g} = \frac{(2D+1)}{1-(K_d+1)D-2K_d D^2} \tag{41}$$

The Switch Utilization Factor is

$$SUF = \frac{V_0 I_0}{V_{SW} I_{s(rms)}}$$

Substituting (39) and (40), the SUF is given in (42)

$$SUF = \frac{4-D}{3\sqrt{D}*G} \tag{42}$$

The voltage stress across capacitor C_1 is obtained from (22) and (23) and is given in (43) and (44)

$$\frac{V_{C1}}{V_g} = \frac{(1+2D)V_g(1-D)}{1-D(K_d+1)-2K_d D^2} \tag{43}$$

The voltage stress across capacitor C_2 is given in (44)

$$\frac{V_{C2}}{V_g} = \frac{(1+2D)K_d D}{1-(K_d+1)D-2K_d D^2} \tag{44}$$

The voltage stress across the input diode D_{in} may be ascertained by analyzing Mode 1. The expression shown below is derived based on the results acquired from steady-state voltage analysis.

$$V_{Din} = V_1 + V_{C2} + V_3$$

By further simplifying, the stress across diode D_{in} is given in (45)

$$\frac{V_{Din}}{V_g} = \frac{K_d(2D+1)_i}{1-(K_d+1)D-2K_d D^2} \tag{45}$$

7. DESIGN CONSIDERATION

7.1 Inductor

Assuming that the converter operates in continuous conduction mode (CCM), the required inductor value is calculated. For CCM operation, the average inductor current must exceed half of the peak-to-peak ripple current. The minimum inductance necessary to maintain CCM is given in equation (46):

$$L_1, L_2 \geq \frac{R_0(4-D)(KD+D+1)}{2G^2(1-(K+1)D-2KD^2)} \tag{46}$$

7.2 Capacitor

The estimation of capacitor values requires consideration of the voltage ripple across each capacitor. Ripple voltage analysis is based on the examination of the capacitor current waveforms, as shown in Figure 7(c). For capacitor design, the current through each capacitor during the switch-on interval0- DT_s is considered. The capacitors in the circuit are C, C_1, C_2, and C_o. Specifically, the current through the capacitor C_1, which is connected to the secondary winding of the coupled inductor during the intervalDT_s,is given in Eq. (47).

$$C_1 = \frac{I_2 DT_s}{\%r_{C1} V_{C1}} \tag{47}$$

where r_{c1} is the ripple percentage of C_1. The current value of Capacitor C_2 during 0-DT_s is $3I_L$as given in Eq. (48)

$$C_2 = \frac{3I_L DT_s}{\%r_{C2} V_{C2}} \tag{48}$$

where, r_{c2} is the ripple percentage of C_2.
The current through the capacitorC in the SLC module during the interval DT_s is $I_L/3$,and the corresponding capacitor value is provided in equation (49)

$$C = \frac{I_L D T_s}{3\% r_C V_C} \quad (49)$$

where $r_C$is the ripple percentage of C.
The current through the output capacitor C_o during DT_s is I_o and the capacitor value C_0 is given in (50).
The current by C_o during the off time (1-D) Ts is as follows:

$$C_0 = \frac{(1-D)T_s I_0}{\%r_{C0} V_{C0}} \quad (50)$$

where r_{C0} is the percentage of ripple allowed in C_o.

8. EFFICIENCY OF THE PEOPOSED CONVERTER

The efficiency of the proposed converter largely depends on its constituent components. Energy losses occur in the diodes, inductors, and switches. The following sections detail the power losses associated with each switch in the system.

8.1 Inductors

The losses due to inductors are of two types: core and copper loss.

$$Pinductor = PC + PCu$$

The core loss is given by (51):

$$P_C = 71.93 * B^{1.92} f_{SW}^{1.47} V_{cv} \quad (51)$$

where B is the flux in the material and V_{CV} is core volume.
The inductor copper loss is due to the average current through the inductor and is given by

$$P_{cu} = I_L^2 R_L$$

The copper loss can be obtained by substituting the average inductor current asgiven in (52)

$$P_{cu} = \frac{(2D+1)V_g I_0^2 R_L}{(4-D)(1-(K_d+1)D-2K_d D^2)} \quad (52)$$

8.2 Diodes

Diode losses can be categorized into three types: forward voltage drop loss, conduction loss, and reverse recovery loss due to trapped charge. The loss caused by trapped charge is negligible and therefore neglected in the analysis. The forward voltage drop loss is expressed in equation (53), while the conduction loss is given in equation (54).

$$P_{forwardvoltage} = (I_{D1A} + I_{D2A} + I_{DinA} + I_{D0A})V_F$$

From (30),(33),(34), we have:

$$P_{forward} = (\frac{(1-D)I_0}{K_d D} + \frac{2K_d I_0}{D} + I_0)V_F \quad (53)$$

$$P_{conduction} = (I_{D1R}^2 + I_{D2R}^2 + I_{DinR}^2 + I_{D0R}^2)I_F$$

From (31),(32),(35)|, we have:

$$P_{conduction} = (\frac{K_d(1-D)I_0}{\sqrt{1-D}})^2 + 2(\frac{K_d I_0}{\sqrt{D}})^2 + (\frac{I_0}{\sqrt{D}})^2)I_F \quad (54)$$

The value of forward voltage (V_F) and forward current (I_F)can be obtained from the data sheet.

8.3 Switches

The switch losses are of two types: conduction loss and switching loss.The losses are represented as Equations in (55) and (56)

$$P_{conduction} = I_{SW}^2 R_{SW}$$

$$P_{conduction} = (\frac{I_0}{\sqrt{1-D}})^2 * R_{sw} \quad (55)$$

The switching losses in a power converter are determined by analyzing the turn-on and turn-off durations of the switches, along with the switching frequency.

$$P_{switch} = \frac{t_{on}+t_{off}}{2} f_{swp} V_{swp} I_{swp} \quad (56)$$

Therefore, the overall power loss is calculated using (57):

$$P_{Loss} = P_L + P_{Diode} + P_{Switch} \quad (57)$$

8.4 Efficiency calculations

For efficiency calculations,the following parameter values were used: r_L=0.15Ω, r_{C1}=r_{C2}=r_C=0.01Ω, r_{c0}=0.12Ω, the on state MOSFET resistance is 0.008mΩ, and the forward voltage drop in diode is V_F=0.7V. The on-state resistance of the diode is 0.01Ω. For an input voltage of 12volts, duty cycle 18%, and a power rating of 100W, the calculated component losses are as follows: inductor loss: Power losses in inductor P_L=3.025W, losses in capacitors P_C=0.75W, losses in diodes in P_D=2.25W, and losses in switch 1.98W. Based on the above losses, the efficiency is 88.8%. Figure 10 presents a pictorial representation of the losses in each component.

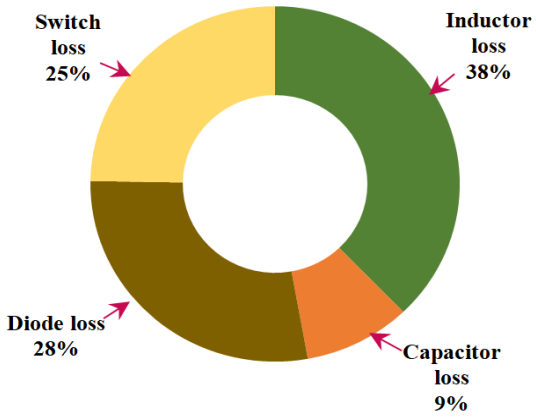


Figure 10. Loss calculations

9. RELIABILITY ANALYSIS

Reliability refers to the ability of a system to perform as expected under standard operating conditions. The key parameter used for reliability assessment is the Mean Time To Failure (MTTF), which is calculated based on the environmental conditions using the military handbook (MIL-HDBK_217F) [30].
The specifications of the components considered for this analysis are provided in Table 2. Figure 11 illustrates the number of components in the converter used for reliability evaluation. According to [30], the failure rate of a component is

$$\lambda_{component} = \lambda_b \sum_{i=1}^{k} \pi_k.$$

where λ_b signifies the component base failure value and k denotes the value of Π factors responsible for failure. The failure of any component in general is given by (58)

$$\lambda_{component} = \lambda_b \pi_T \pi_A \pi_Q \pi_E \quad (58)$$

Here,λ_b denotes the base failure, π_T is the temperature value, π_A is the application value, π_Q is the quality value, and π_E denotes the environmentvalue.The components under consideration are switch, diodes, inductors, and capacitors. Total failure in the case of the proposed converter is

$$\lambda_{converter} = \lambda_{switch} + \lambda_{diode} + \lambda_{inductor} + \lambda_{capacitor}$$

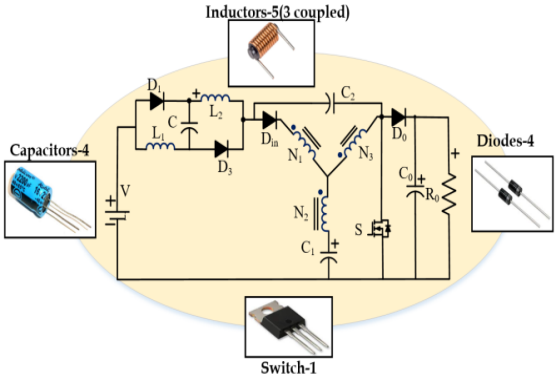


Figure 11. Number of components used for reliability evaluation

Table 2. Specifications used for reliability analysis

Component	Rating
Switch	IRF 630, Voltage/ Current[200V/10A], Junction to case temperature-θ_{JC}=1.7C/W, On state resistance-$R_{ds(on)}$=0.4Ω, output capacitance=240pF
Diode	Schottky,MBR 10 100CT,Voltage/Current[100V,5A], junction to case temperature θ_{JC}=4C/W, Internal resistance R_i=0.15Ω
Capacitor	Electrolytic, Fixed and Aluminium
	Voltage /Current [100V,5A],Capacitance10-30μF,Resistance=0.2 to 0.5Ω, 200 V,5A, Resistance=1Ω
Inductors	200μH,6A, Inductive resistance R_L=0.350mΩ, 300μH,6A, inductive resistance R_L=0.800mΩ

9.1 Switch failure rate

The rate of failure of switch is given by:

$$\lambda_{switch} = \lambda_b \pi_T \pi_A \pi_Q \pi_E \text{ failures}/10^6\text{hours.}$$

where π_A is the application factor, representing the usage conditions of the application at a power rating of 100 W. The values of π_E, π_A, and π_Q are obtained from the MIL-HDBK_217F handbook and are presented in Table 3. The environment considered for this analysis is ground-mounted (Gm). The value of π_T is:

$$\pi_T = (-1925(\frac{1}{J+273}) - (\frac{1}{298})) \text{ and } J = T_C + \theta_{JC}.P_{SW}$$

where J is the junction temperature,the case temperature is T_C, $P_{SW}$is the switch losses, and θ_{JC} denotescaseto junction temperature. The value of λ_{SW}obtained by substituting the values is 8.2752 failures/106hours.

Table 3. Pi factors of the switch used for calculations

Component	λ_b	π_T		π_A	π_Q	π_E	
		Gm	AUC			Gm	AUC
Switch	0.012	1.92	2.89	4	5.5	9	20

9.2 Diode failure rate

The rate of failure of diode is given by:

$$\lambda_{diode} = \lambda_b \pi_E \pi_T \pi_C \pi_S \pi_Q \text{ failures}/10^6\text{hours.}$$

Where π_S is the stress factor,which is obtained from handbook[30] and presented in Table 4. π_C is the contact construction factor. It depends on the type of bonding required to make contact with PCB. The value of π_T is

$$\pi_T = (-3091(\frac{1}{J+273}) - (\frac{1}{298}))$$

$$J = T_C + \theta_{JC}.P_D$$

where J is the junction temperature, $T_C$denotes case temperature value; P_D is the diode power loss, and θ_{JC} is the case and junction temperature. The value of λ_D obtained is 0.8612 failures/10^6hours.

Table 4. Pi factors of the diode used for calculations

Component	λ_b	π_T		π_S	π_Q	π_E		π_C
		Gm	AUC			Gm	AUC	
Diode	0.003	4.37	7.92	1.204	2.4	9	20	1

9.3 Inductor failure rate

The rate of failure of inductor is given by:

$$\lambda_{inductor} = \lambda_b \pi_Q \pi_E \pi_C \text{ failures}/10^6 \text{ hours.}$$

The π factors used for reliability evaluation are presented in Table 5. The base failure rate (λ_b)for the inductor is considered for Class C insulation with an operating temperature above 125°C and is given as $\lambda_b = 0.00035 \exp \exp (\frac{\Delta T+273}{409})^{10}$. The value of λ_L obtained by substituting the values is 0.06384failures/10^6hours.

Table 5. Pi factors of the diode used for calculations

Component	λb	πQ	πE		πC
			Gm	AUC	
Inductors	3.694*10^-4	1	12	6	1

9.4 Capacitor failure rate

The rate of failure of capacitor is given by:

$$\lambda_{capacitor} = \lambda_b \pi_Q \pi_E \pi_{CV} \text{ failures}/10^6 \text{ hours.}$$

$\lambda_b$for capacitor is

$$\lambda_b = 0.000254((\frac{V_R}{0.5})^3 + 1) \exp(5.09(\frac{T+273}{358})^5)$$

where V_R is the ratio of working to rated voltage. π_{CV} is the capacitance valuewhich is obtained on the basis of dielectric used in the capacitors. The value of $\lambda_C$obtained by substituting the values is 0.1699 failures/106hours.

Table 6. Pi factors of the capacitors used for calculations

Component	λ_b	π_{CV}	π_E		π_Q
			Gm	AUC	
Fixed, electrolytic aluminium capacitor	0.168	0.7	12	28	0.03

9.5 Mttf calculation

The mean time taken to fail is calculated using (59) as follows:

$$\text{MTTF} = \frac{1}{\lambda_{switch}+\lambda_{diode}+\lambda_{inductor}+\lambda_{capacitor}}. \quad (59)$$

10. COMPARISONS WITH OTHER IMPEDANCE SOURCE NETWORKS

This section presents a comparative analysis of the proposed converter and other Y-source converters. The winding factor K_d is set to 3. Table 3 provides a comprehensive overview of the key characteristics of the proposed converter.

10.1 Comparisons of voltage gain

Figure 12 illustrates the variation of voltage gain with respect to duty cycle for different converters reported in the literature. It is evident from the figure that the proposed converter achieves a higher voltage amplification compared to other Y-source converters documented previously.

10.2 Comparisons of voltage stress

Figure 13(a) illustrates the voltage stress experienced by the capacitors in various Y-source converters. The analysis indicates that the proposed converter exhibits a significant reduction in capacitor stress compared to most existing Y-source converters. This reduction directly enhances the

reliability of the converter. Although the converters reported in(Siwakoti, Y. P. et al., 2016) and (Wang, Y. et al., 2019) also demonstrate low capacitor voltage stress, they suffer from discontinuous input current and limited voltage gain. Figure 13(b) shows the voltage across the diodeD_{in},which is considerably lower than that observed in other converters documented in the literature.

10.3 Comparisons of component count

Table 7 presents a comparison of the component count between the proposed converter and those reported in the literature. The proposed topology uses fewer components than the SL Y-source converter as shown in Figure 14. Although conventional Y-source and quasi-Y-source converters employ even fewer components, the proposed converter offers the advantages of higher voltage gain and continuous input current, providing a superior balance between performance and complexity.

Table 7. Comparison of SLC Y-source converter with the existing converters in the literature

Parameter		Siwakoti, Y. P et al., 2014	Siwakoti, Y. P et al., 2015	Siwakoti, Y. P. et al., 2016	Wang, Y. et al., 2019	Yuan,J.et al.,2020)	Proposed
Components	L	1	2	1	2	2	2
	C	2	3	3	2	4	3
	Sw	4	1	1	1	1	1
	Diodes	3	3	4	5	3	4
	Total	10	9	9	10	10	10
Voltage Gain		$\frac{K_d+2}{1-D}$	$\frac{1}{1-(K_d+1)D+K_dD^2}$	$\frac{1+K_d-D}{(1-D)^2}$	$\frac{1}{1-(2+K_d)D}$	$\frac{1+D}{1-(1+K_d)D-K_dD^2}$	$\frac{1+2D}{1-(1+K_d)D-2K_dD^2}$
Gain K_d=3,D=0.18		6	12	5.9	10	7	16
Maximum voltage when input is 12		72	144	70.8	120	84	192

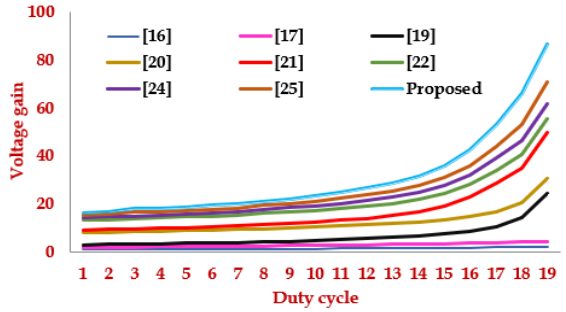


Figure 12. Voltage gain for different converters for different duty ratios with winding factor 3

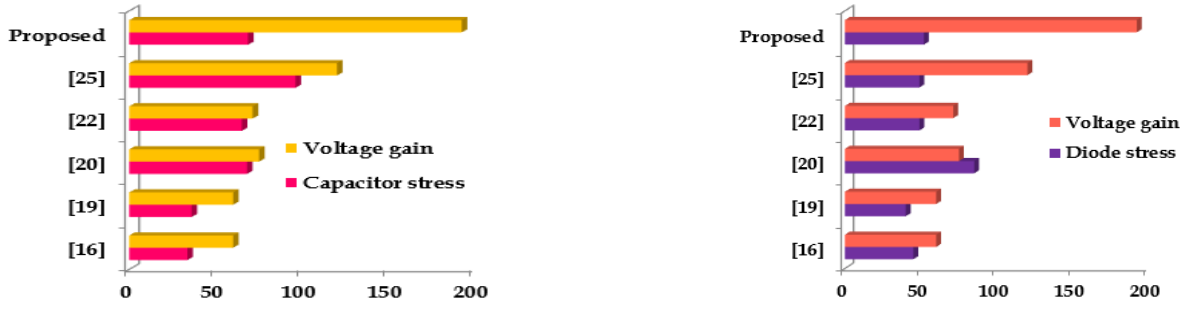


Figure 13. (a)Comparison of capacitor voltage across capacitor with converter in literature (b) Comparison of capacitor voltage across diodes with converters in literature

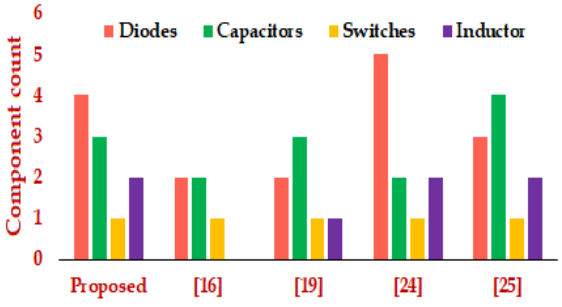


Figure 14. Comparison of the component count of the converter.

10.4 Comparisons of component count

The proposed converter is compared with the topology reported in (Wang, Y. et al., 2019)in terms of reliability, as summarized in Table 8. For an input voltage of 12 V, a power rating of 100 W, and a winding factor of 3, the following comparative analysis is presented. Table 8 presents the comparative results obtained from the reliability and efficiency analysis. From these results, it is evident that replacing the diode D2 with a capacitor C significantly enhances the performance of the proposed converter.

Table 8. Reliability and Efficiency comparison of the proposed converter with the converter suggested byWang Y. et al. (2019)

Parameter	SLY source	Proposed
Input voltage	12	12
Duty cycle	20%	18%
Max. Output voltage	180V	192V
Efficiency	85.3%	88.8%
Reliability	94.6khr	104.14 Khr
Diode failure rate	1.35 failures/10^6 hours	0.93 failures/10^6 hours
Percentage decrement in diode failure	**45%**	

11. SIMULATION AND EXPERIMNTAL RESULTS

Table 9 summarizes the parameters used for the experimental verification. A photograph of the prototype and the experimental setup is shown in Figure 15.

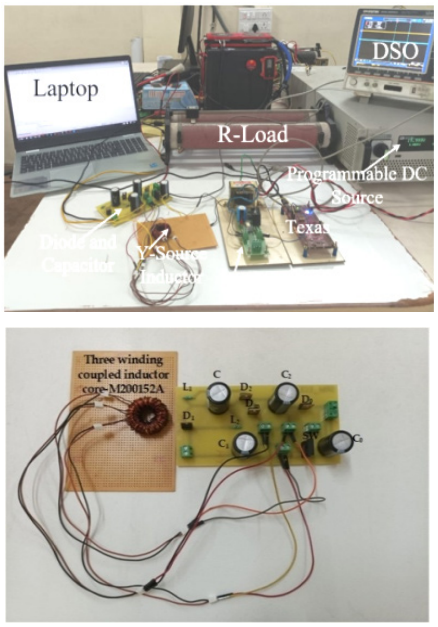


Figure 15. Photograph of the experimental setup

TABLE 9: The Proposed Converter Specifications

Parameters	Specifications
Input Voltage (V_{dc})	12 V
Power rating (P_o)	100W
Capacitor C_1andC_2	330 µF, 100µF,
Capacitor C and C_0	115µF,336µF
Switching Frequency (f_r)	20 kHz
L_1 and L_2	800 µH
Load	R=200 Ω
N_3 :N_2 :N_1	50:20:40; $\mathbf{k_d}$=3
D	18%
Switch	IRF630
Diode D_1	MBR10

The performance of the proposed converter was evaluated using MATLAB/SIMULINK, and experimental validation was carried out on a 100 W prototype. The DC input voltage to the converter was Vg = 12 V, with an operating frequency of 20 kHz. The prototype was specifically constructed and tested for duty ratios of D = 0.18 (18%), D = 0.15 (15%), and D = 0.10 (10%), with a turns ratio set to K = 3.

11.1 Simulation results

The simulation of the proposed topology was conducted using MATLAB/Simulink. The simulation parameters were set as follows: Vg = 12 V, fs = 20 kHz, Kd = 3, C1 = C2 = C = 330 µF, and L1 = L2 = 800 µH. Figures 16(a)–16(i) present the simulation results.

- Figure 16(a) shows the input voltage, Vg = 12 V.
- Figure 16(b) depicts the output voltage of the converter at a duty cycle of D = 18%, which reaches 190 V.
- Figure 16(c) illustrates the switch voltage, Vsw, which is equivalent to 180 V since the switch is connected across the load.
- Figure 16(d) shows the voltage across capacitor C2, VC2 = 96 V.
- Figure 16(e) presents the input diode voltage, VDin = 38 V.
- Figure 16(f) shows the voltage across capacitor C1, VC1 = 76 V
- Figure 16(g) displays the voltage across diodes D1 and D2, V = 26 V.
- Figure 16(h) and 16(i) depict the input current, Iin = 8.6 A, and the output current, I0 = 0.48 A, respectively.

11.2 Transient analysis

The transient analysis of the proposed topology is carried out. The performance of the converter under changes in input voltage and load is simulated and presented in Figure 17. The response of the converter when the input voltage is varied from 6 V to 12 V is shown in Figure 17(a). As illustrated, when the source voltage is 12 V, the load voltage is approximately 96 V, and the output current is around 0.35 A, while the source current is approximately 4 A. When the input voltage is increased from 6 V to 12 V, the output voltage rises to about 188 V, and the load current increases to 0.48 A. The input current rises to 8.3 A.

Due to the sudden change in input voltage, the source current experiences a minimum peak before settling.The response of the circuit elements to a sudden change in load is shown in Figure 17(b). As the load increases, both the load voltage and current decrease, whereas the source current increases. Owing to the sudden variation in load, the source current experiences a minimum peak before stabilizing.

11.3 Experimental results

The results of the experimental prototype are depicted in Figure 18(a)–(f). The output voltage is obtained for duty cycles of d = 0.1 (10%), d = 0.15 (15%), and d = 0.18 (18%). The winding factor is set as Kd = 3, and the DC input to the converter is Vg = 12 V. From Figure 18(a), it is observed that when the input voltage (Vin) is 12 V and the duty ratio (d) is 0.1, the resulting output voltage is 27 V. As shown in Figure 18(b), when the duty ratio is increased to d = 0.15, the output voltage rises to 59 V.

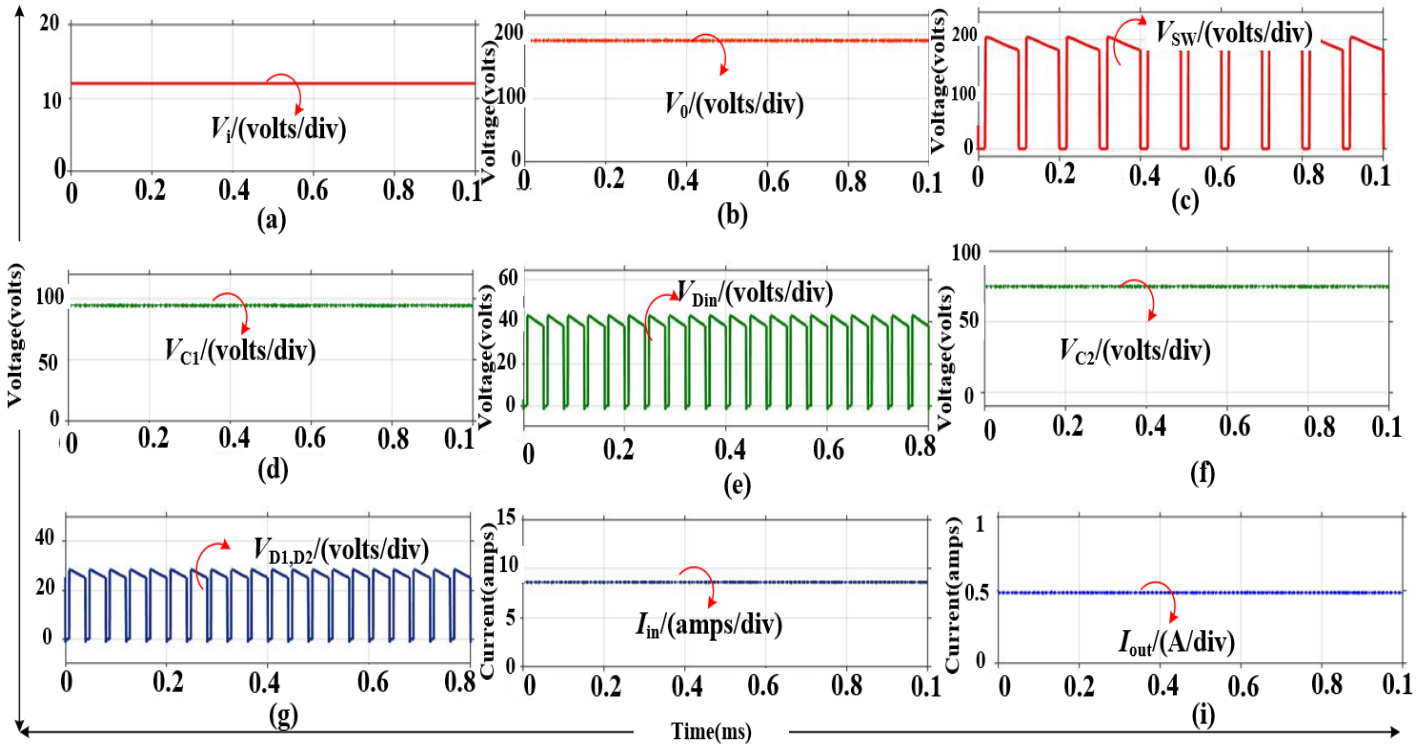


Figure 16. (a) Source voltage; (b) Output voltage with k_d=3 and D=0.18; (c) Switch voltage; (d) Capacitor voltage V_{C2}; (e) Diode voltageV_{Din}; (f)Capacitor voltage V_{C1}; (g) Diode voltage $V_{D1,2}$;(h)Input current; (i) Output current

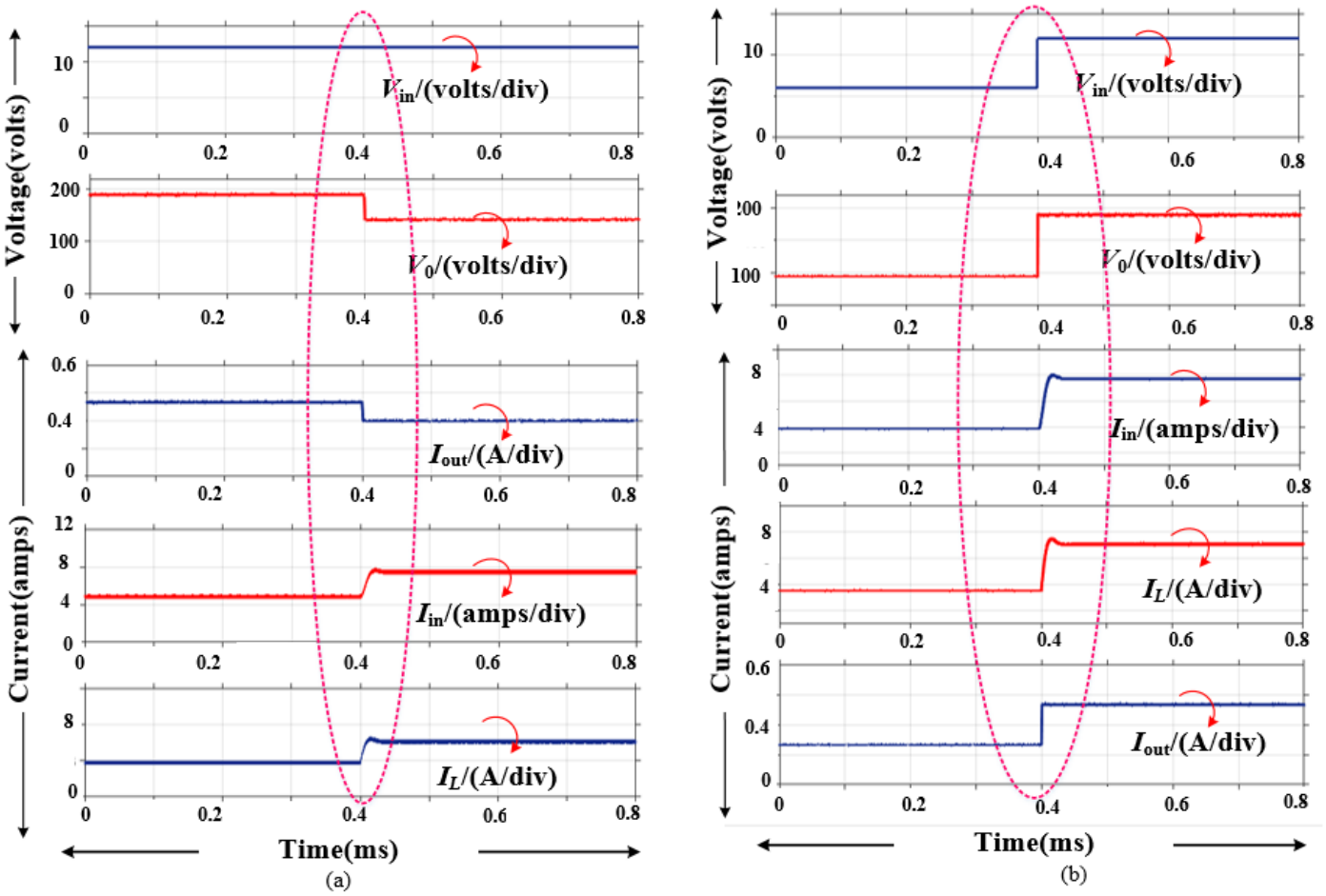


Figure 17. Performance of converter (a) Change in load; (b) Change in source.

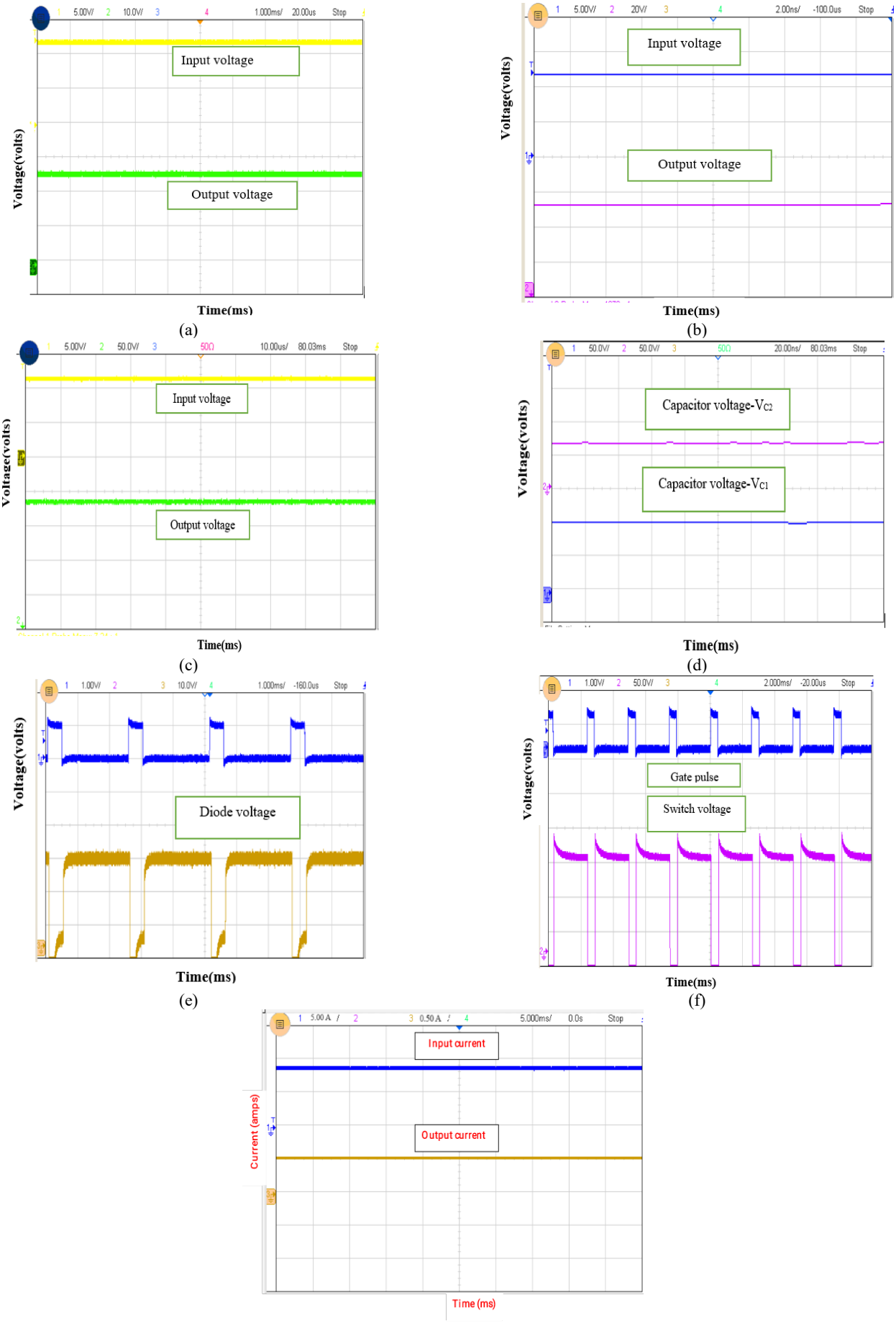


Figure 18. (a)Input and output voltage with K=3 and D=0.1; (b)Input and output voltage with K=3 and D=0.15; (c) Input and output voltage of with K=3 and D=0.18; (d)Capacitor voltages V_{C1} and V_{C2} of the converter; (e)Voltage across the diodes D_1 and D_2; (f)Voltage across the switch SW and the pulse input to the MOSFET gate (g)Input and output current

When the duty ratio is set to d = 0.18, the resulting output voltage of the converter is 189 V, as shown in Figure 18(c). The voltages across the capacitors, VC1 and VC2, are 101 V and 79 V, respectively, as depicted in Figure 18(d). The voltage across the switch is presented in Figure 18(f) and is equal to the output voltage of 185 V. The input and output currents are 8.3 A and 0.5 A, respectively, as shown in Figures 18(f) and 18(g).

Based on these results, it is evident that an increase in the duty ratio leads to a higher gain of the converter while maintaining a constant winding factor Kd. Although the converter's gain increases with higher duty ratios, operating at elevated duty cycles may result in increased losses.

12. CONCLUSION

In this article, a Y-source converter with an SLC boost module is proposed and analyzed. A detailed steady-state investigation is performed for the proposed Y-source converter. The following points highlight the significant characteristics of the converter.

- As the duty ratio decreases, the duration of current flow through the switch is reduced. Consequently, the reduction in power loss within the switch enhances the reliability of the converter.
- Figure 13 illustrates that the proposed converter achieves a significantly higher voltage gain compared to both conventional and improved Y-source converters, all operating under the same turn-on duty ratio.
- Equation (26) shows a positive correlation between the voltage gain and the winding factor of the converter, indicating the design's adaptability.
- At a duty cycle of 18%, the converter achieves a gain 16 times the input voltage.
- The inclusion of a switched inductor-capacitor module ensures continuous input current. Moreover, the capacitor connected in parallel with the inductor helps mitigate the effects of inrush current, making the converter suitable for PV applications.

The dynamic behavior of the proposed topology will be analyzed using small-signal analysis, followed by the design of a controller for load regulation.

13. ACKNOWLEDGEMENT

The authors sincerely thank the authorities of the respective universities and institutes for their support of this research.

NOMENCLATURE

PV	=	Photo Voltaic
LCT	=	Inductor Capacitor Transformer converter
K	=	Winding factor
D	=	Duty ratio
N_1,N_2,N_3	=	Turns ratio of the three-winding transformer
K_{cric}	=	Critical inductance
CCM	=	Continuous Conduction Mode
DCM	=	Discontinuous Continuous Conduction Mode
SUF	=	Switch Utilization Factor

Data Availability Statement: The datasets used and/or analyzed during the current study available from the corresponding author upon reasonable request.

REFERENCES

1. Adamowicz, M. (2011). LCCT-Z-Source Inverters. 1*0th International Conference on Environment and Electrical Engineering*. 1-6. https://doi.org/10.1109/EEEIC.2011.5874799
2. Anitha, P., Kumar, K. K. & Kamaraja, A.S,.(2023). An Improved Design and Performance Enhancement of Y-Source DC-DC Boost Combined Phase Shifted Full Bridge Converter for Electric Vehicle Battery Charging Applications. *Journal of Electrical Engineering Technology.18*.2983–2996. https://doi.org/10.1007/s42835-023-01414-1
3. BabayiNozadian, M., Babaei, E., Hosseini, S. H., &Shokati A. E. (2019). Switched Z-Source Networks: A Review. *IET Power Electronics. 12.* https://doi.org/10.1049/iet-pel.2018.5436
4. Buticchi, G., Lam, C. S., Xinbo, R., Liserre, M., Barater, D., Benbouzid, O., and Bellmunt,G. (2021). The Role of Renewable Energy System in Reshaping the Electrical Grid Scenario. *IEEE Open Journal of the Industrial Electronics Society, 2*,451-468. https://doi.org/10.1109/OJIES.2021.3102860
5. Cao, C. & Peng, F.Z. (2009). A Family of Z-source and Quasi-Z-source DC-DC Converters.*Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, Washington, DC, USA,* 1097-1101. https://doi.org/10.1109/APEC.2009.4802800.
6. Chub, A., Vinnikov, D., Blaabjerg, F., & Peng, F. Z.(2015). A review of galvanically isolated impedance-source dc-dc converters. *IEEE Transactions on Power Electronics*, 31(4), pp. 2808-2828. https://doi.org/10.1109/TPEL.2015.2453128
7. Forouzesh, M., Siwakoti, Y. P., Gorji, S. A., Blaabjerg, F., & Lehman, B.(2017). Step-Up DC–DC Converters: A Comprehensive Review of Voltage-Boosting Techniques, Topologies, and Applications. *IEEE Transactions on Power Electronics, 32(12),* 9143-9178, https://doi.org/10.1109/TPEL.2017.2652318.
8. Ji, Y., Liu, H., Feng, Y., Wu, F. & Wheeler, P.(2020). High Step-Up Y-Source Coupled-Inductor Impedance Network Boost DC-DC Converters With Common Ground and Continuous Input Current. *IEEE Journal of Emerging and Selected Topics in Power Electronics. 8(3).* 3174-3183. https://doi.org/10.1109/JESTPE.2019.2892499
9. Liu, H., Ji, Y., Wang, L., & Wheeler, P.(2018). A Family of Improved Magnetically Coupled Impedance Network Boost DC–DC Converters. *IEEE Transactions on Power Electronics*.33(5). 3697-3702. https://doi.org/10.1109/TPEL.2017.2763153
10. Liu, H., Ji, Y., Zhang, C., & Wheeler, P. (2018). A Family of High Step-Up Coupled-Inductor Impedance-Source Inverters With Reduced Switching Spikes. *IEEE Transactions on Power Electronics*. 33(11).9116-9121. https://doi.org/10.1109/TPEL.2018.2820814.
11. Liu, H., Li, Y., Zhou, Z., & Wu, H. (2019). A Modified Y-Source Inverter. *2019 IEEE Applied Power Electronics Conference and Exposition (AEC)*.3477-3482. https://doi.org/10.1109/APEC.2019.8722155
12. Loh, P. C., Li, D. & Blaabjerg, F. (2013). Γ-Z-source inverters. *IEEE Transactions on Power Electronics. 28(11).* 4880-4884. https://doi.org/10.1109/TPEL.2013.2243755
13. Peng, F. Z. (2003). Z-source inverter. *IEEE Transactions on Industry Applications.39(2).* 504-510. https://doi.org/10.1109/TIA.2003.808920
14. Reddivari, R., & Jena, D. (2019). Novel Active Clamped Y-Source Network for Improved Voltage Boosting.*IET Power Electronics.* 205-2014. https://doi.org/10.1049/iet-pel.2018.6212
15. Shahir, F. M., Babaei, E., and Farsadi, M. (2019). Extended Topology for a Boost DC–DC Converter. *IEEE Transactions on Power Electronics.34(3),*2375-2384. https://doi.org/10.1109/TPEL.2018.2840683
16. Shen, H., Zhang, B., & Qiu, D. (2017). Hybrid Z-Source Boost DC-DC Converters.*IEEE Transactions on Industrial Electronics. 64(1).* 310-319. https://doi.org/10.1109/TIE.2016.2607688
17. Siwakoti, Y. P., Blaabjerg, F. & Loh, P. C. (2015). Quasi-Y-Source Boost DC-DC Converter. *IEEE Transactions on Power Electronics.30(12).*6514- 6519. https://doi.org/10.1109/EPE.2015.7311678
18. Siwakoti, Y. P., Blaabjerg, F. ,Galigekere V. P., Ayachit, A., & Kazimierczuk, M. K.,(2016). A-Source Impedance Network. *IEEE Transactions on Power Electronics.31(12).*8081-8087. https://doi.org/10.1109/TPEL.2016.2579659
19. Siwakoti, Y. P., Blaabjerg, F., & Loh, P. C.(2016). New Magnetically Coupled Impedance (Z-) Source Networks. *IEEE Transactions on Power Electronics. 31(11).*7419-7435. https://doi.org/10.1109/TPEL.2015.2459233

20. Siwakoti, Y. P., Loh, P. C., Blaabjerg, F., & Town, G. (2014). Y-source impedance network. *IEEE Applied Power Electronics Conference and Exposition*.3362-336. https://doi.org/10.1109/TPEL.2013.2296517

21. Siwakoti, Y. P., Loh, P. C., Blaabjerg, F., Andreasen, S. J., & Town, G. E. (2015). Y-Source Boost DC/DC Converter for Distributed Generation. *IEEE Transactions on Industrial Electronics, 62(2).* 1059-1069. https://doi.org/10.1109/TIE.2014.2345336

22. Siwakoti, Y. P., Peng, F. Z., Blaabjerg, F., Loh, P. C., & Town, G. E.(2015). Impedance-Source Networks for Electric Power Conversion Part I: A Topological Review. *IEEE Transactions on Power Electronics.30(2).*699-716. https://doi.org/10.1109/TPEL.2014.2313746

23. Soon, J. J., & Low, K. -S. (2014). Sigma-Z-source inverters. *IET Power Electronics.8(2).* 637-746. https://doi.org/10.1049/iet-pel.2014.0274

24. Strzelecki, R., Adamowicz, M., Strzelecka, N. & Bury, W. (2009). New type Tsourceinverter.*Proceedings of. CPE.* 191-195. https://doi.org/10.1109/CPE.2009.5156034

25. Sugali, H., & Sathyan, S.(2023). Design and analysis of isolated high step-up Y-source DC/DC resonant converter for photovoltaic applications, *Energy Sources, Part A: Recovery, Utilization, and Environmental ffects.45(1).*16041623. https://doi.org/10.1080/15567036.2023.2179698

26. Wang, Y., Wenli, J., Yuping, Q., Yuanyuan, W., Xiangyuan, D., Hua, K., Hu, B.,& Xu, D. (2019). A Family of Y-Source DC/DC Converter Based on Switched Inductor. *IEEE Transactions on Industry Applications.55(2).* 1587-1597. https://doi.org/10.1109/TIA.2018.2871658

27. Yang, Y., Enjeti, P., Blaabjerg, F., & Wang, H.(2015).Wide-scale adoption of photovoltaic energy: Grid code modications are explored in the distribution grid. *IEEE Industry Applications*, 21(5), pp. 21-31. https://doi.org/10.1109/MIAS.2014.2345837

28. Yuan, J., Mostaan, A., Yang, Y., Siwakoti, Y. P., & Blaabjerg, F.(2020). A Modified Y-Source DC-DC Converter With High Voltage-Gains and Low Switch Stresses. *IEEE Transactions on Power Electronics*. 35(8).7716 – 7720. https://doi.org/10.1109/TPEL.2020.2964153